A MODERN HYBRID COMPUTER INTERFACE

by

Jeffrey Martin Wilkins

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ABSTRACT

This paper discusses the hybrid linkage system which interfaces the LOCUST high speed iterative differential analyzer and the PDP-9 digital computer to form a hybrid computing system. The interface comprises four analog-to-digital converters and four multiplying digital to analog converters for data transfer between computers. A control register, read-in gates and patchable flags provide digital control functions in the linkage. PDP-9 loaded counters and PDP-9 timing signals also add flexibility to the interface. Patching instructions and input/output transfer instructions which control the interface are discussed. An amplitude distribution example utilizing the interface demonstrates a type of problem that may be handled with the linkage.

CHAPTER I

INTRODUCTION

The LOCUST-PDP-9 interface was designed and constructed in the University of Arizona's Computer Science Research Laboratory. The purpose of this hybrid linkage is to enable the LOCUST high-speed analog computer and the PDP-9 digital computer each to perform the functions they are best able to perform while maintaining an interaction that makes the combination much more powerful than either machine working alone. The high-speed differential-equation solving ability of the analog computer is maintained and the accuracy, memory, and decision making ability of the digital computer are added.

LOCUST (LOw CoST) is a high-speed solid-state interative differential analyzer capable of operating at iteration rates as high as 4000 analog computer runs per second as well as in real time (Conant, 1968). It employs flexible digital control logic as well as patchable free logic. Provision was made at the time of LOCUST's construction for the addition of control logic driven from a digital computer. All of the digital logic in LOCUST is MECL emitter-coupled integrated circuit logic, chosen for its low noise.

The Digital Equipment Corporation PDP-9 programmed data processing system is a general purpose computer, incorporating diode-transistor negative logic throughout. It is a single-address, fixed-word-length (18 bits), parallel binary computer. The PDP-9 has a

1 μ sec complete cycle time. (PDP-9 User Handbook, Digital Equipment Corporation, 1968).

I/O Operation

The basic PDP-9 I/O facilities utilized for the LOCUST-PDP-9 interface include;

1. An I/O bus system which chain links all the device controls for all peripheral devices to the central processor unit.
2. A program interrupt control.
3. An I/O status read provision.
4. A conditional skip-on-device-status sense line provision.

The I/O bus consists of command lines and bidirectional data lines for use in accomplishing program-controlled transfers; plus the program interrupt control, the I/O status read, and conditional skip-on-device-status provisions. Detailed information on the PDP-9 I/O system is contained in the PDP-9 User Handbook (Digital Equipment Corporation, January, 1968).

Under construction is a data-channel interface for block transfers to and from the PDP-9 memory.

General Description of the Interface

The two essential functions of the interface are: data transfer between computers and control of the analog computer by the digital

computer. The primary data-transfer devices are four analog-to-digital converters (ADCs) and four multiplying digital-to-analog converters (MDACs). The remaining data transfer devices are 6 data read-in gates and a 6-bit control register. The read-in gates and the control register enable the operator to transfer discrete logic levels to and from the PDP-9 accumulator (AC) under program control. Control functions are generated both by the PDP-9 and LOCUST. At the present time, there are two patchable flags in LOCUST which are connected to the Program Interrupt (PI) and Skip Request (SKIP) lines of the PDP-9, with provision made for four more. Programmable IOT pulses gated by a device selector are brought out in LOCUST as well as other useful PDP-9 generated signals; IO SYNC, IO RUN, POWER CLEAR, and ENABLE. Two 10-bit binary counters located in LOCUST serve as "alarm clocks" preset by the digital computer; each counter can count patchable LOCUST-generated pulses and generate timing and sampling signals. A block diagram of the interface is shown in Fig. 1. The level converters (MECL/DEC, DEC/MECL) indicated in the figure are discussed in Chapter II.

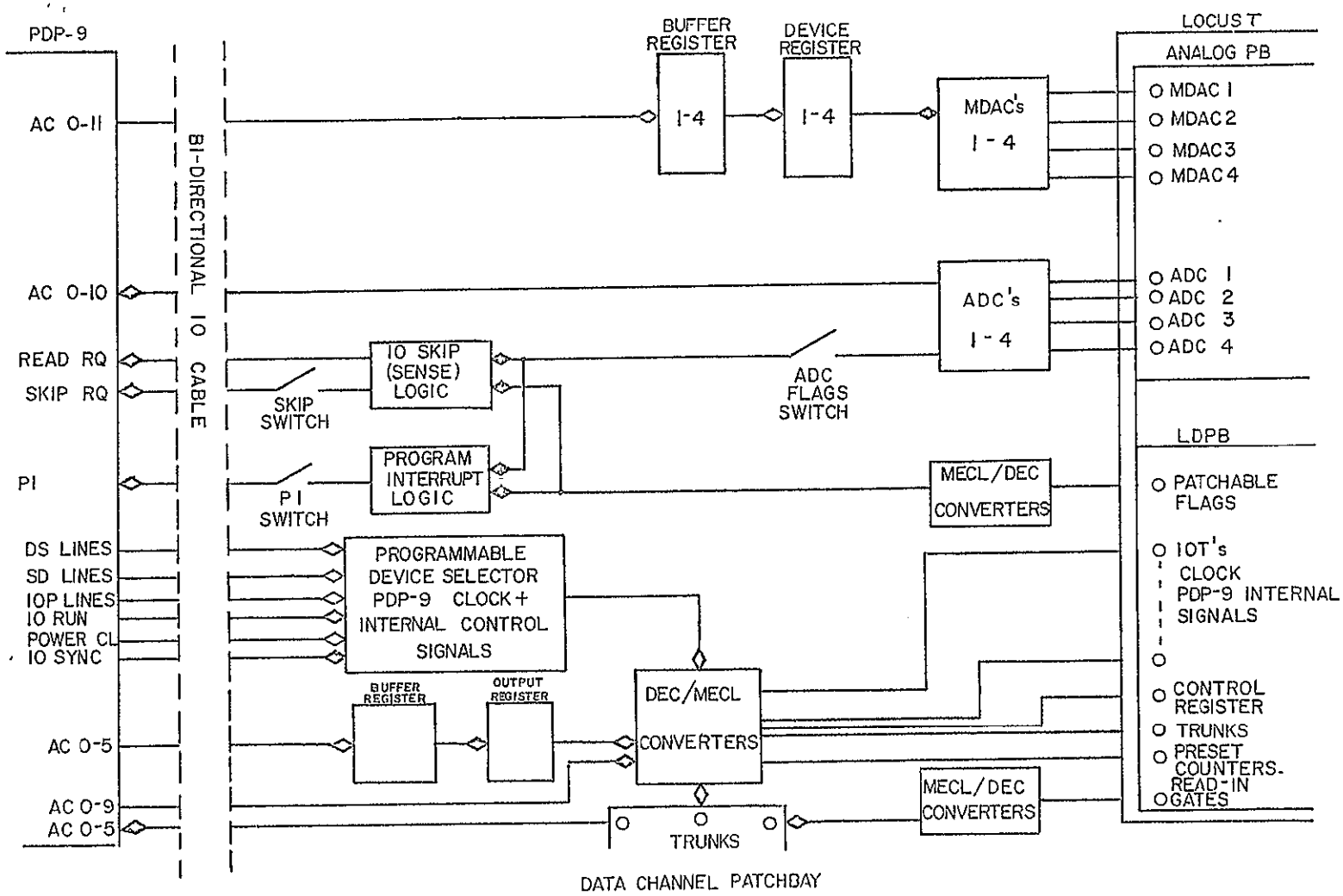


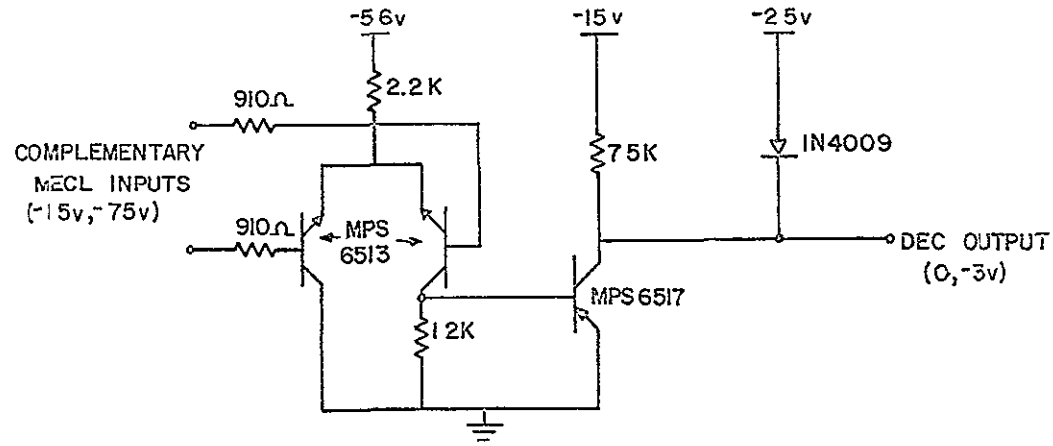
Fig. 1 Block Diagram of the Interface

CHAPTER II

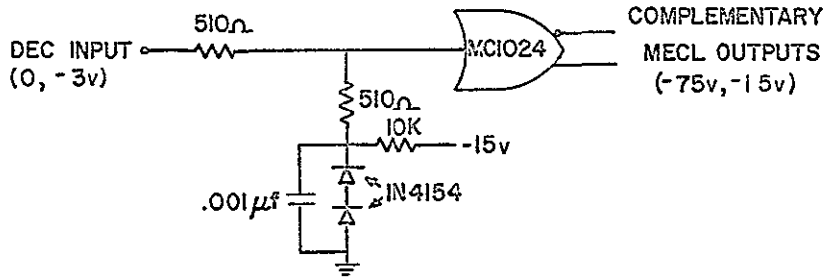
DETAILED CIRCUIT DESCRIPTION

The LOCUST/PDP-9 interface comprises essentially two sections. One section contains DEC logic (0 v, -3 v logic levels) and is located in three DEC Type 1943 mounting panels attached to a standard 19-inch rack cabinet, which makes up the left hand bay of the LOCUST machine. The other section contains MECL II current mode logic (-.75 v, -1.5 v logic levels) and is located on printed-circuit cards which plug into the back of the LOCUST digital patchbay (LDPB). Conversion of logic levels is made by MECL/DEC (Goltz, 1968) and DEC/MECL converters on standard DEC cards that plug into the Type 1943 mounting panels (Fig. 2). All signals passing between the DEC portion of the logic and the MECL portion of the logic do so at MECL levels via twisted pairs. A twisted pair is driven by the complementary outputs of any MECL device; each pair is terminated by an MC1020 line receiver with a 100 ohm shunt resistor. The resulting low-impedance line assures high noise immunity. The MECL/DEC converters also serve as line receivers, making an MC1020 unnecessary. MECL II was chosen for use in LOCUST because of its inherent low noise stemming from its balanced-current, nonsaturating operation.

With the use of the MECL trunking scheme it is possible to drive line lengths limited only by series resistance, propagation



(a)



(b)

1. ALL RESISTORS ARE 1/2W 10%

Fig. 2 (a) MECL/DEC Converter

(b) DEC/MECL Converter

delay, and common-mode noise. The twisted pairs used in the LOCUST-PDP-9 interface are eight feet long.

The location of the DEC logic is shown in Fig. 3. The location of a logic card is identified by a letter(row) and a number(column). The pins are lettered. The MECL logic is located on three plug-in cards lettered A, B, and C and two counter cards lettered D and E mounted in brackets behind the LOCUST digital patchbay. The individual integrated circuits are numbered as are the pins. The MECL logic layout for cards A, B, and C and the card placement in the patchbay is shown in Fig. 4. The counter logic layout is shown in Fig. 5. The logic symbols used throughout the interface diagrams are shown in Fig. 6.

All of the DEC flip flops used in the interface use DCD gates except for the simpler set-reset flip flops used in the flag logic. If the input level of a DCD gate is at ground at least 400 nsec prior to a -3 v to 0 v transition at the pulse input, the flip flop will trigger.

Device Selector Operation

Device Selectors (See Fig. 7) decode the device-address bits of each IOT instruction word and gate (IOP/IOT) pulses to effect desired data transfers, skip tests, or other device operations. In the LOCUST / PDP-9 interface, a single device selector is used for both an ADC and an MDAC. Device-selector IOT pulses are gated with subdevice bits from the PDP-9 to provide the necessary pulses.

WIRING SIDE

	A	B	C	D	E	F
32	R202		K_5	K_8	K_1	K_3
31	R202	R202	K_4	K_7	M/D	K_2
30	R203	R203	R202	K_6	M/D	M/D
29	RII3	R603	R202	R202	D/M	M/D
28	RII3	RII3	R202	R202	D/M	M/D
27	WI03A	WI03B	R203	R202	D/M	M/D
26	WI03A	WI03B	R203	R203	D/M	D/M
25		W640	R603	R203	D/M	D/M
24			RI23	RI23	R200	R200
23			W640	RI23	R603	R200
22			RII3	RI07	R603	R603
21			WI03A	WI03B	RIII	RI07
20			SECONDARY BUS	SECONDARY BUS		RIII
19			SECONDARY BUS	SECONDARY BUS	R202	R202
18			W500	W500	R202	R202
17			PRIMARY BUS	PRIMARY BUS	R202	R202
16			PRIMARY BUS	PRIMARY BUS	R203	R200
15			RII3	RI07	R203	
14			WI03A	WI03B	R203	RI23
13			W640	RI07	R203	RII3
12			R603	RI23	WI03A	WI03B
11			R203	RI23	WI03A	WI03B
10			R203	RI23	R603	W640
9			R203	RI23	R203	RII3
8		RII3	R203		R203	RI23
7			R202	R202	R203	RI23
6			R202	R202	R203	RI23
5			R202	R202	R202	R202
4	K_{16}		K_{12}		R202	R202
3	K_{15}		K_{11}		R202	R202
2	K_{14}		K_{10}	RI23	R200	R603
1	K_{13}		K_9	R200		RI07

Fig. 3 DEC Logic Layout

VIEW FROM GROUND PLANE

SIDE OF CARDS

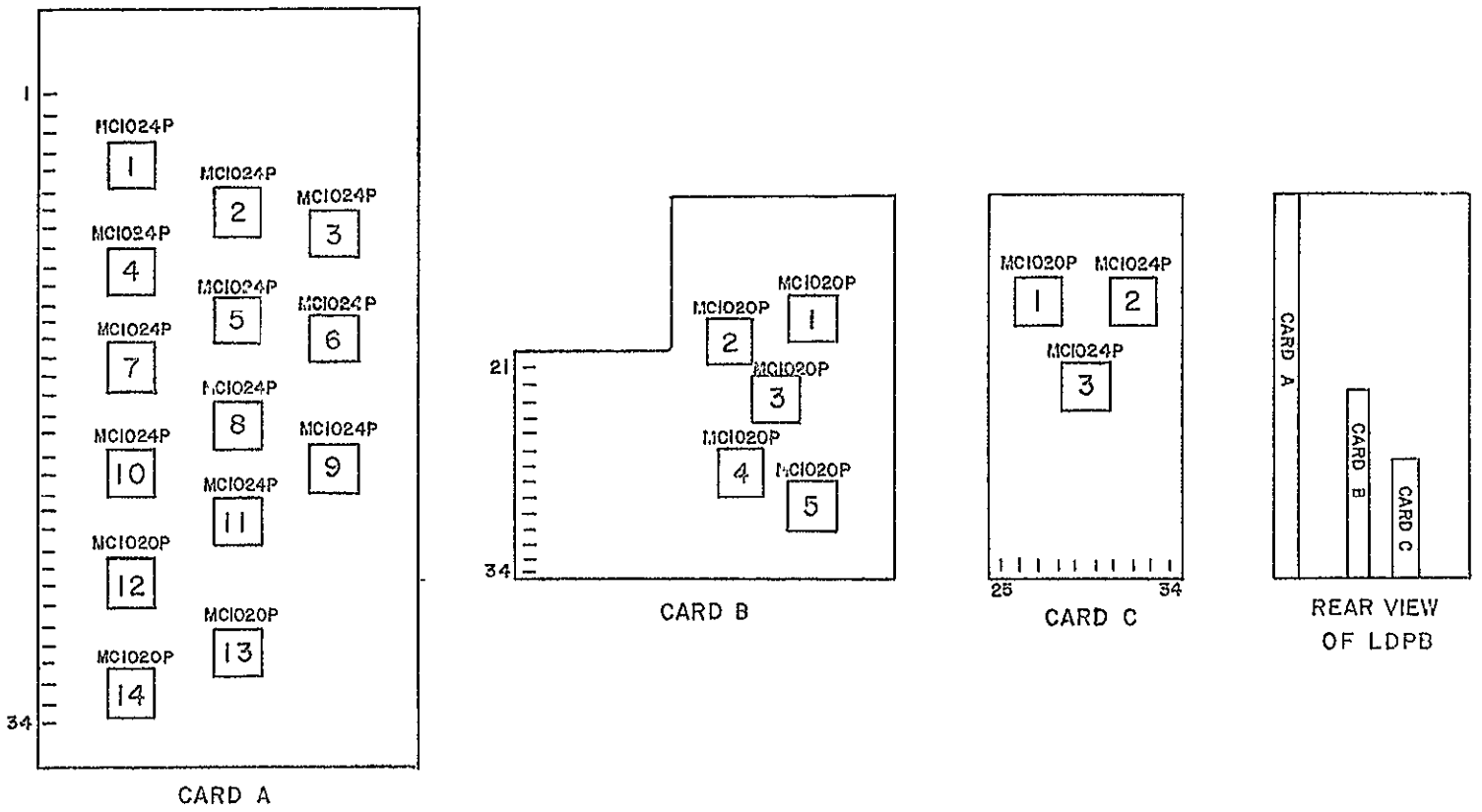
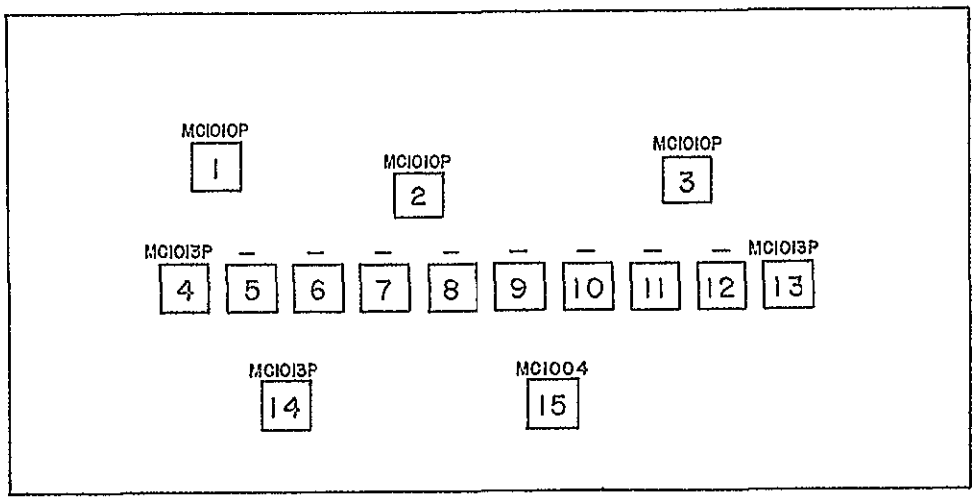


Fig. 4 MCC Logic Layout



VIEW FROM GROUND PLANE SIDE

Fig. 5 Counter Logic Layout

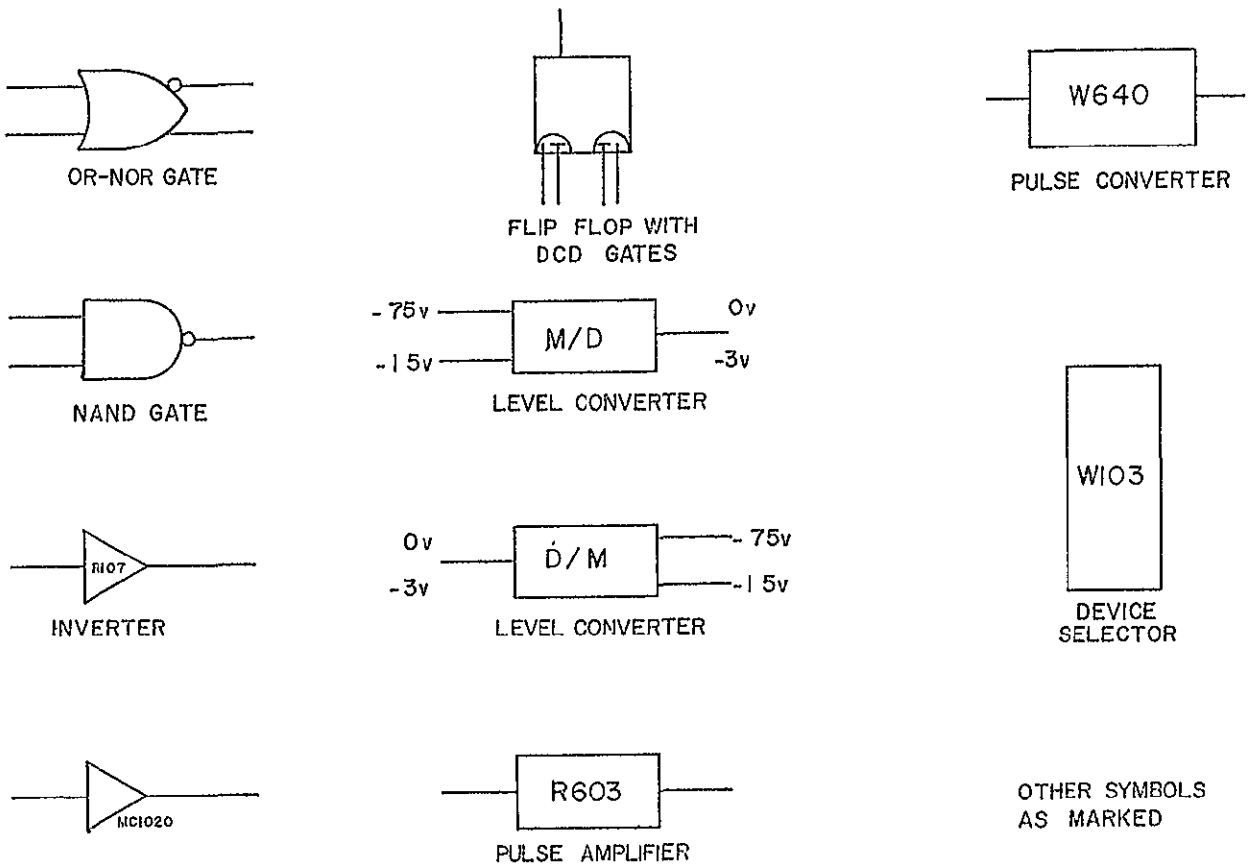


Fig. 6 Logic Symbols

Flag Logic

There are presently four ADC flags and two patchable flags in the interface. The ADCs have a status indicator output, which is at ground if the converter is busy and at -3 v when a conversion is complete. This output is used to set and reset a DEC R200 flip flop, which serves as the "flag". This flag may also be cleared by the ADC read pulse and the PDP-9 POWER CLEAR signal. The patchable flag inputs from the LDPB are trunked to the DEC logic and converted to DEC levels by MECL/DEC converters. The converter outputs set and reset their respective flag flip flops. These flags may also be cleared by a programmable IOT pulse and IO POWER CLEAR. A representative section of flag logic is shown in Fig. 7.

The ADC status indicator goes to -3 v when a conversion is complete. This signal is inverted to provide a positive going pulse at the diode input of an R603 pulse amplifier. The output of the pulse amplifier is a positive going 100 nsec pulse which sets the flag (flip flop) to a -3 v. A read IOT pulse is gated with IO POWER CLEAR and inverted to provide a positive going pulse to the diode input of a pulse amplifier connected to the reset input of the flag. A DCD gate on the same pulse amplifier is enabled with a ground input and pulsed with the device status indicator to reset the flag. Hereafter, the word "flag" means the output of the respective R200 flip flop.

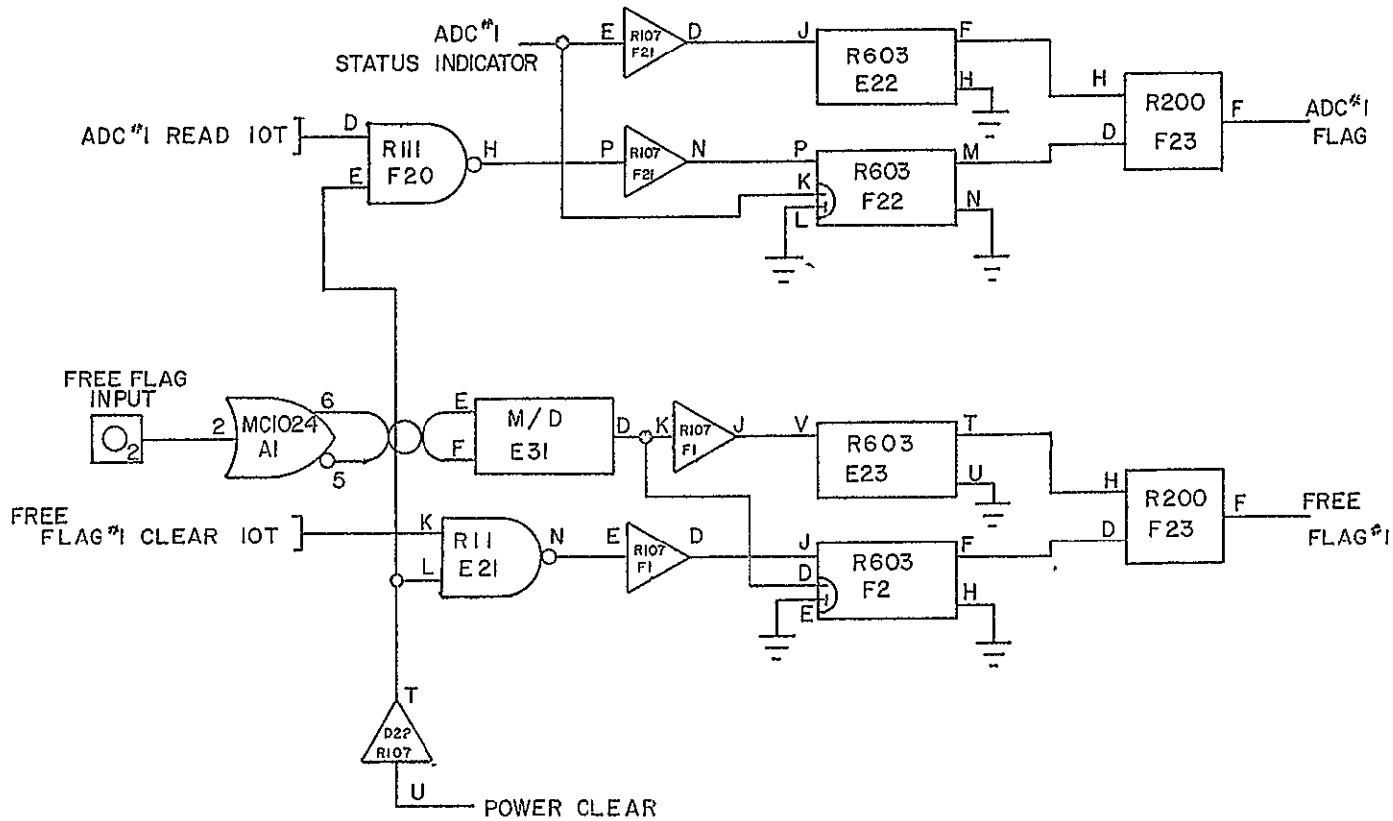


Fig. 7 Flag logic

ADC Data Transfer

The four-channel analog-to-digital converter was designed and built by John R. Goltz. It is an 11 -bit two's-complement converter with parallel binary output. Conversion time is between 50 and 270 μsec. Detailed information on the ADC is contained in ACL Memo No. 147 (Goltz, 1968). Unless otherwise noted, all signals discussed in this section refer to Fig. 8.

When an A/D conversion is completed, a flag is raised which is connected through a gate to the PI line of the IO bus. When the PDP-9 receives a PI signal, it immediately begins looking for the source of the interrupt. The PDP-9 interrupt-service routine issues a series of IOT pulses which are gated with the flags of peripheral devices to the SKIP line. When the raised flag is tested and a skip request is granted, the PDP-9 then executes a service subroutine corresponding to that specific flag. This subroutine reads the converter by gating the converter output onto the IO bus with an IOT pulse. This same read IOT pulse is connected to the READ REQUEST line and is also used to clear the converter flag. The READ REQUEST tells the PDP-9 to read the data that is on the IO bus into the AC. Upon completion of the service subroutine, the PDP-9 returns to the main program. Detailed information on programming the PDP-9 input-output system is contained in the PDP-9 User Handbook (Digital Equipment Corporation, January, 1968). There are four identical sections of ADC

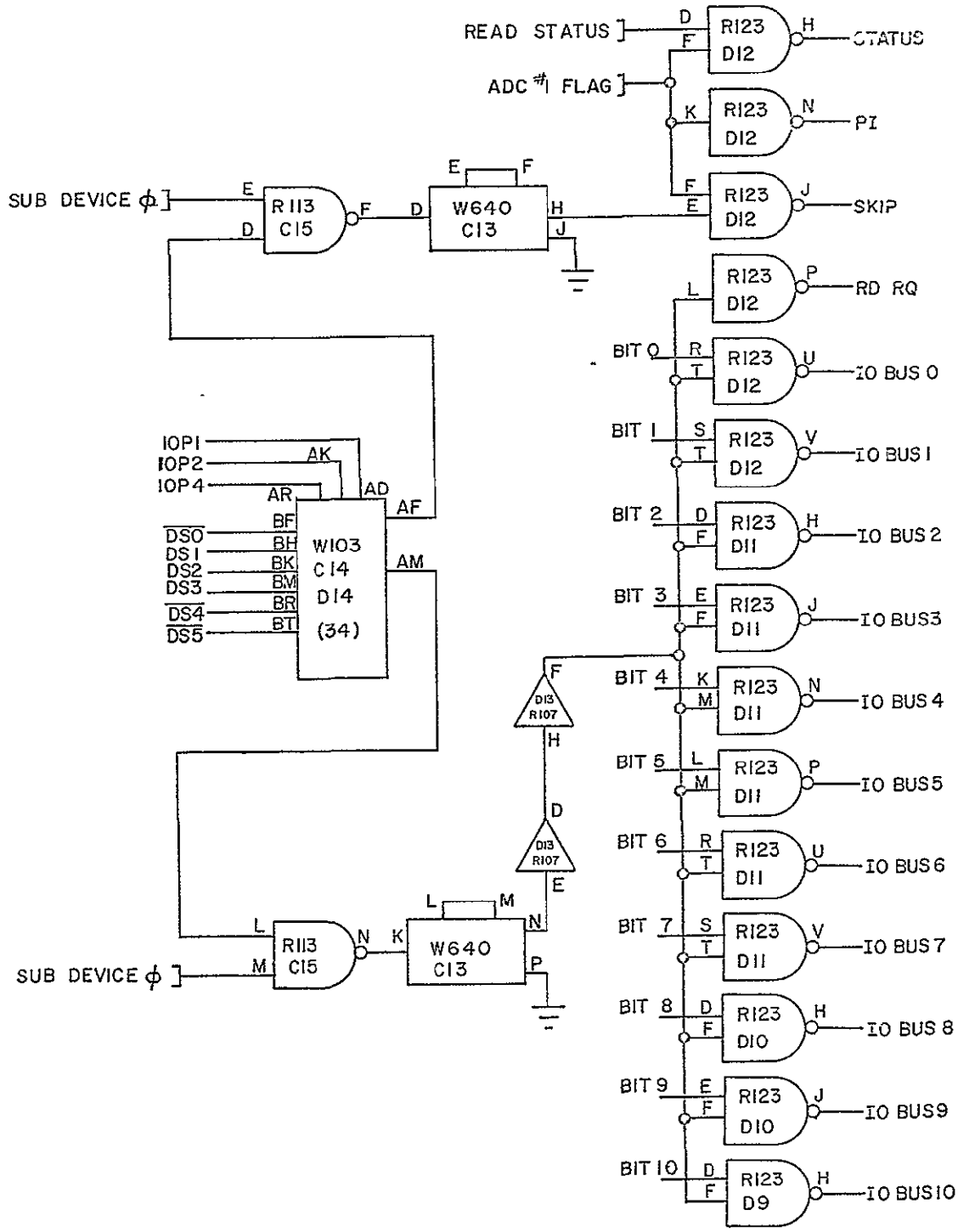


Fig. 8 ADC Logic

logic, hence only one section is shown in Fig. 8. The number in parentheses in the W103 device selector block is the device address octal code.

The ADC converter flag is connected through an inverter to the PI line. A negative going IOT1 pulse from a device selection is gated with negative subdevice bit 0 to provide a positive 100 nsec pulse at the input of the pulse converter. The pulse converter is wired to provide a 1 μsec negative pulse at the input of the R123 bus gate. The other input of this nand gate is connected to the converter flag. Hence when the flag is a -3 v and a negative test pulse appears, a ground level is placed on the Skip Request line for 1 μsec. A negative going IOT2 pulse is gated with negative subdevice bit 0 to provide a positive 100 nsec pulse at the input of pulse converter W640. The negative 1 μsec pulse output of the W640 is inverted twice to provide a negative read pulse with the proper drive at the input of the R123 bus gates. The ADC data (negative assertion) is connected to the other inputs of the bus gates and is gated onto the IO data lines as a ground level when the read pulse appears. The read pulse is also inverted through another gate and connected to the READ REQUEST line.

MDAC Data Transfer

The 12-bit two's complement MDACs were developed as a master's thesis by Don C. Eddington (Eddington, 1969). There are four double-buffered MDACs in the LOCUST/PDP-9 interface.

The interface logic for an MDAC consists of a buffer register and a device register. Double buffering permits simultaneous updating of digital inputs to all MDACs. The buffer is first cleared and then loaded with the accumulator contents by a PDP-9 IOT instruction. The buffer-to-device-register jam transfer can be effected either by a PDP-9 instruction or by patching a MECL "1" to a D/A TRANS input in the LOCUST digital patchbay. The use of a jam transfer to load the device register eliminates the undesired transient that would occur at the MDAC output if the device register were cleared prior to each transfer from the buffer register.

There are four identical sections of MDAC logic; for clarity, only one section is shown in Fig. 9. The buffer register, made up of R203 flip flops, is fed data from the IO data lines through W500 emitter followers. The buffer is cleared with IOT1 (gated with PDP-9 subdevice bit 1), a positive-going 100 nsec pulse at the "clear" input of the flip flops. Data from the emitter followers is connected to the level inputs of DCD gates, and the strobe pulse is provided by IOT2 also gated with sub-device bit 1; the strobe signal is power amplified by an R603 pulse amplifier. The R603 provides a positive-going 100 nsec pulse when the positive transition of the gated IOT pulse occurs. Thus, when the data (ground assertion) and the strobe pulse occur at the DCD gates, the buffer is loaded.

Complementary outputs of the buffer-register flip flops are connected to level inputs on corresponding flip flops in the device register. The pulse inputs of the DCD gates on the R202 flip flops

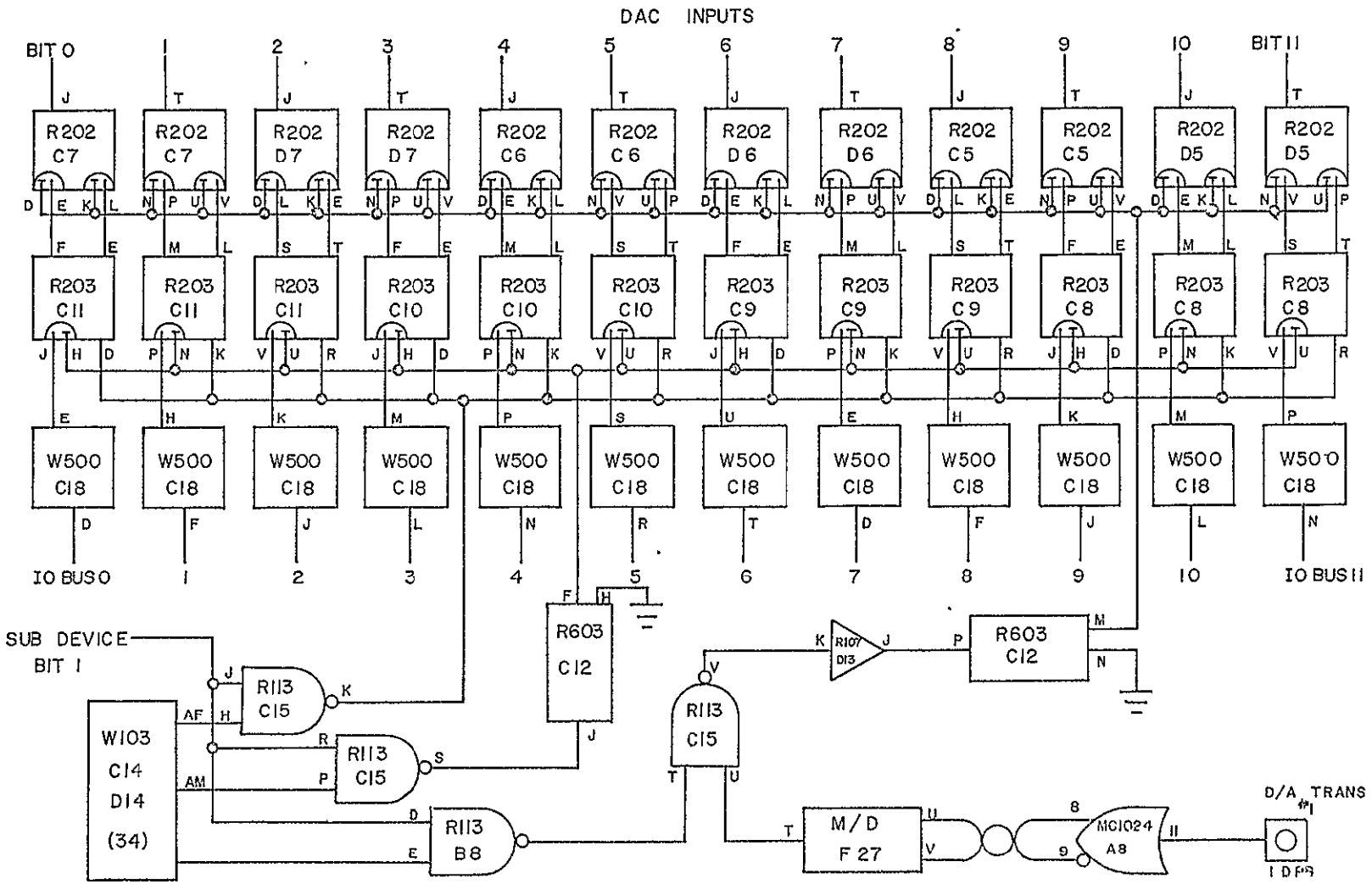


Fig. 9 DAC Logic

are driven with a positive-going pulse from a pulse amplifier. The positive transition at the pulse amplifier input is provided, after inversion, by either a transfer signal from the LOCUST digital patchbay (a MECL/DEC converter output) or IOT4 gated with subdevice bit 1. The MDAC analog switches are connected to the "1" outputs of the R202 flip flops, i.e. -3 v assertion corresponds to an FET switch closure.

Control Register Data Transfer

The six-bit double-buffered control-register logic is similar to the MDAC logic (Fig. 10). The buffer register is cleared by a gated IOT1 pulse. The data is read into the buffer from W500 emitter followers using a gated IOT2 with the proper drive to provide the pulse input to DCD gates. The data is jam transferred into the output register by a gated IOT4 pulse from a pulse amplifier. IO POWER CLEAR clears the output register when the computer is first started. The IO POWER CLEAR signal is issued when the IO RESET switch is depressed on the PDP-9 operating console. The output of the control register is converted to MECL levels and trunked to the LOCUST digital patchbay.

Data Read in Gates

The read-in gate inputs are MECL gate inputs in the LOCUST digital patchbay. The signals are trunked to the DEC logic bay, converted to DEC levels and brought out in the data-channel patchbay (DCPB). There, the outputs are patched into R123 bus gates and data is strobed onto the IO bus with IOT2 from a W103 device selector. A

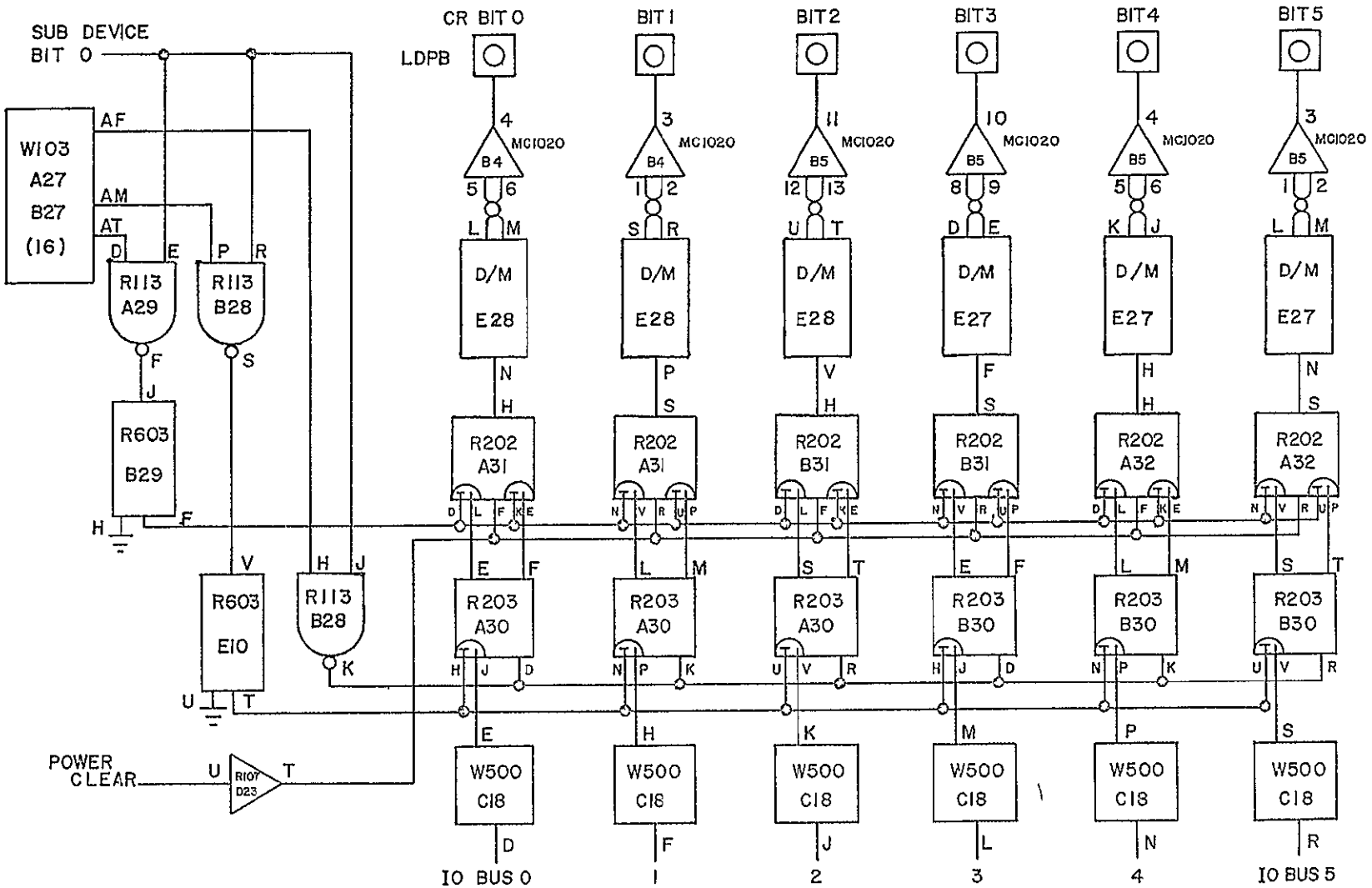


Fig. 10 Control Register Logic

read request must also be made with IOT2. This is accomplished by patching in the DCPB. The read-in gate trunks are shown in Fig. 11a. Maintenance drawings for the gate and device-selector logic are contained in the report on the data channel interface CSRL Memo. 215 (University of Arizona, 1969).

DEC/MECL Trunks

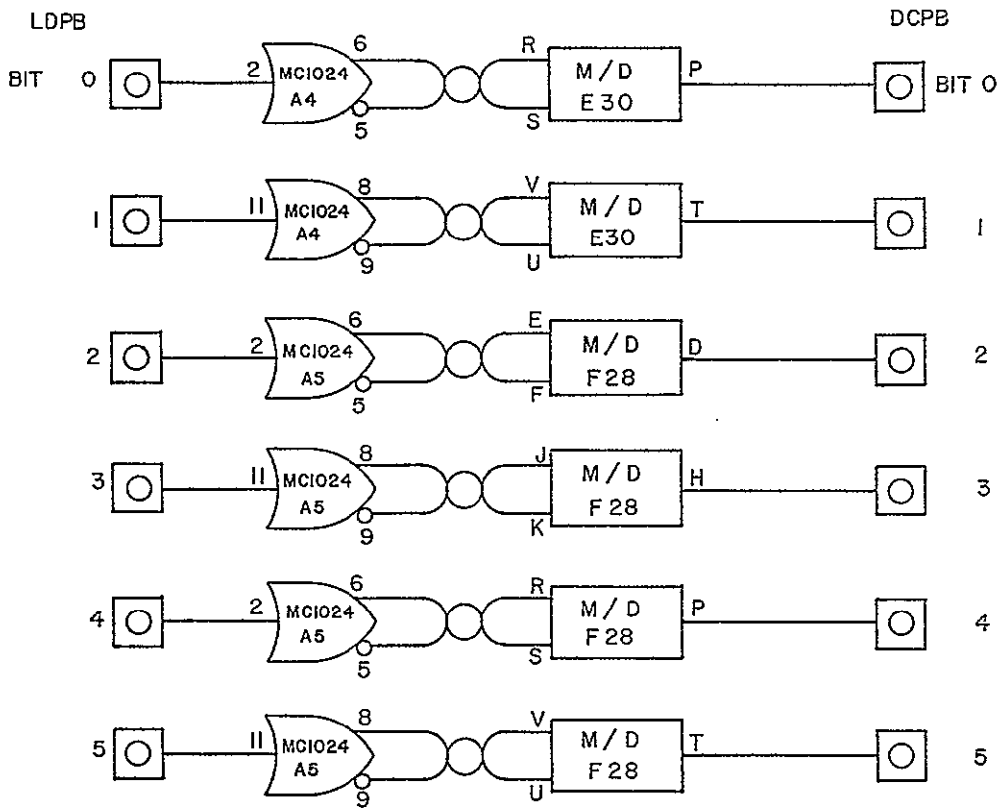
The wiring for four trunks from the data channel patchbay to the LOCUST digital patchbay is shown in Fig. 11b. DEC levels are converted to MECL levels and trunked via twisted pairs.

Oscilloscope Trunks

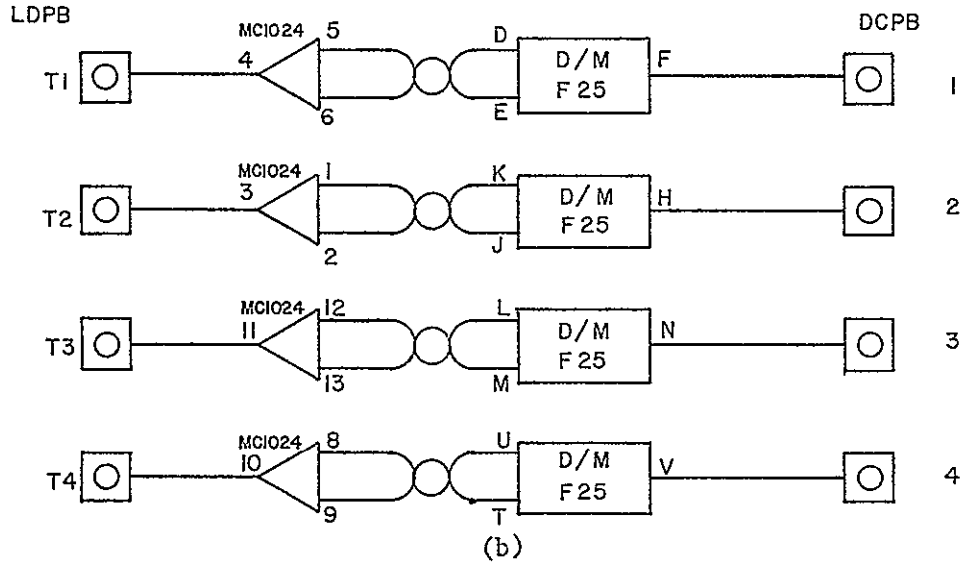
Digital drivers using the standard MECL trunking scheme are also used to provide oscilloscope inputs from the LOCUST digital patchbay.

Preset Counters

Two ten-bit binary counters located in the rack cabinet behind the LDPB are loaded from the PDP-9 upon command. Each MECL counter is a down counter, which is first cleared and then loaded with the complement of one less than the number of pulses to be counted. The counters count LOCUST pulses and issue "S" and "S_D" timing pulses used mainly to operate track hold pairs (Korn and Korn, 1964). A timing diagram is shown in Fig. 12. Discussion of the counter logic refers to Figs. 13, 14 and 15. The two counters are identical except for their operating IOT instructions.



(a)



(b)

Fig. 11 (a) Read-in Gate Trunks (b) DEC/MECL Trunks

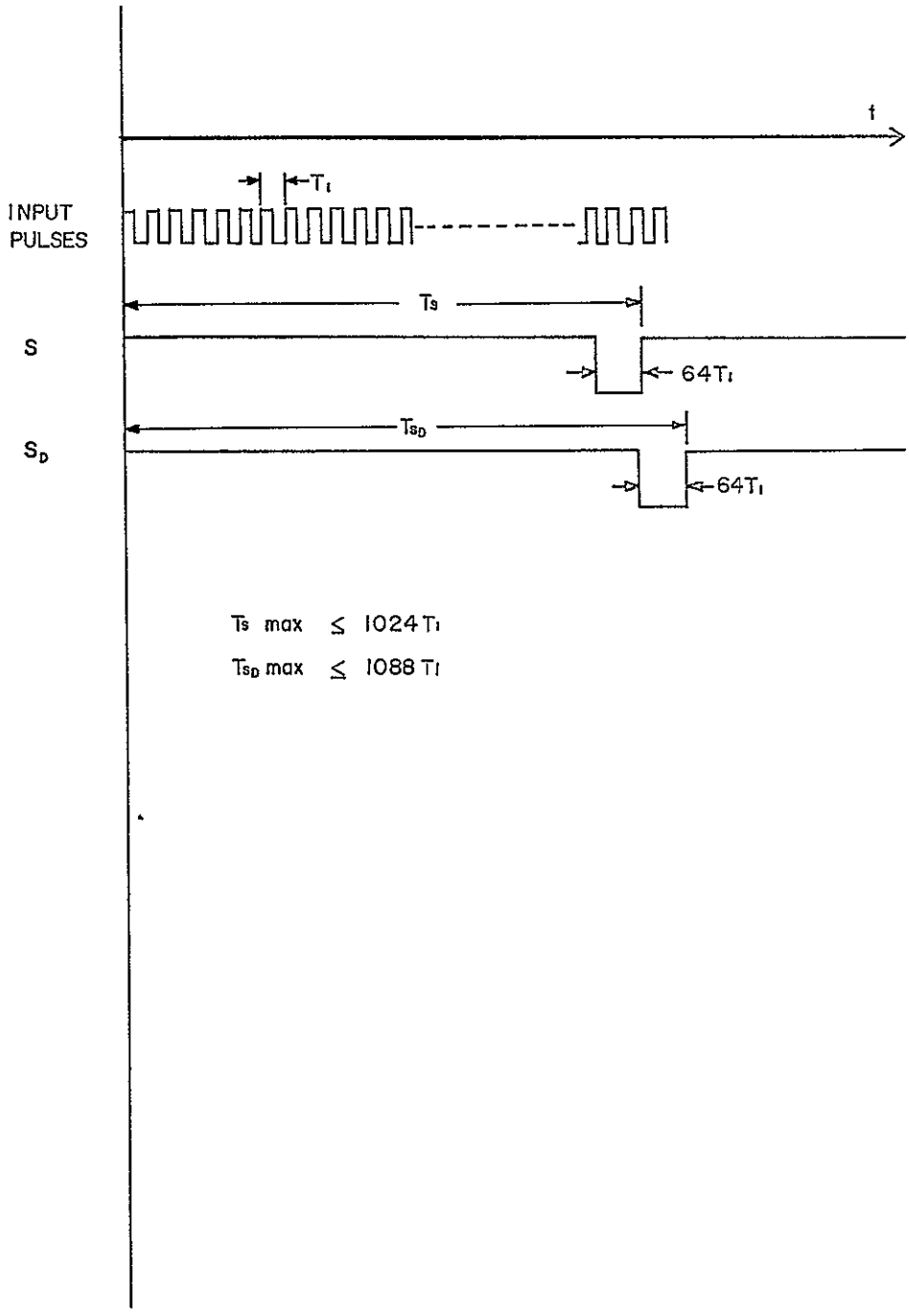


Fig. 12 Preset Counter Timing Diagram

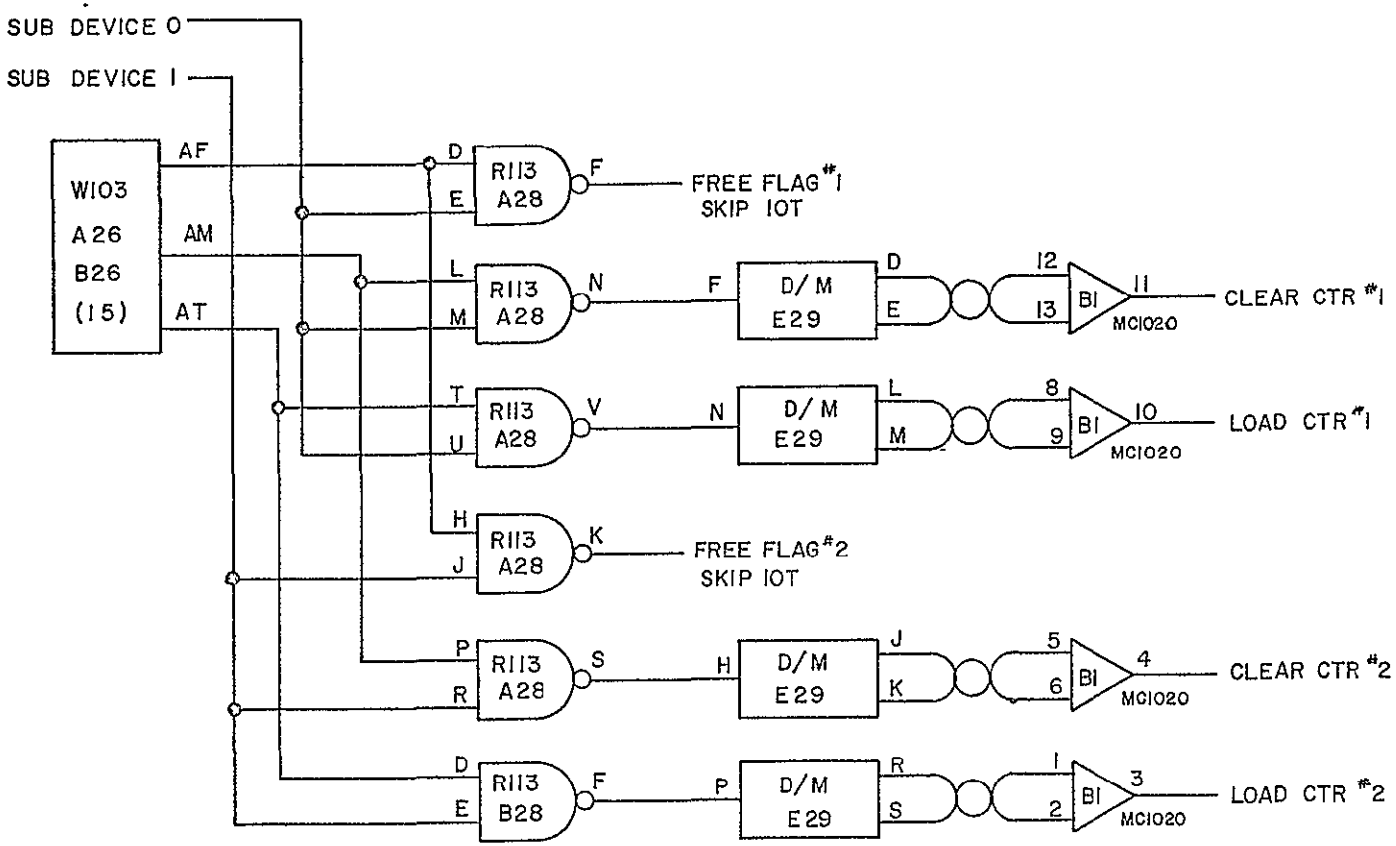


Fig. 13 Preset Counter Control Signals

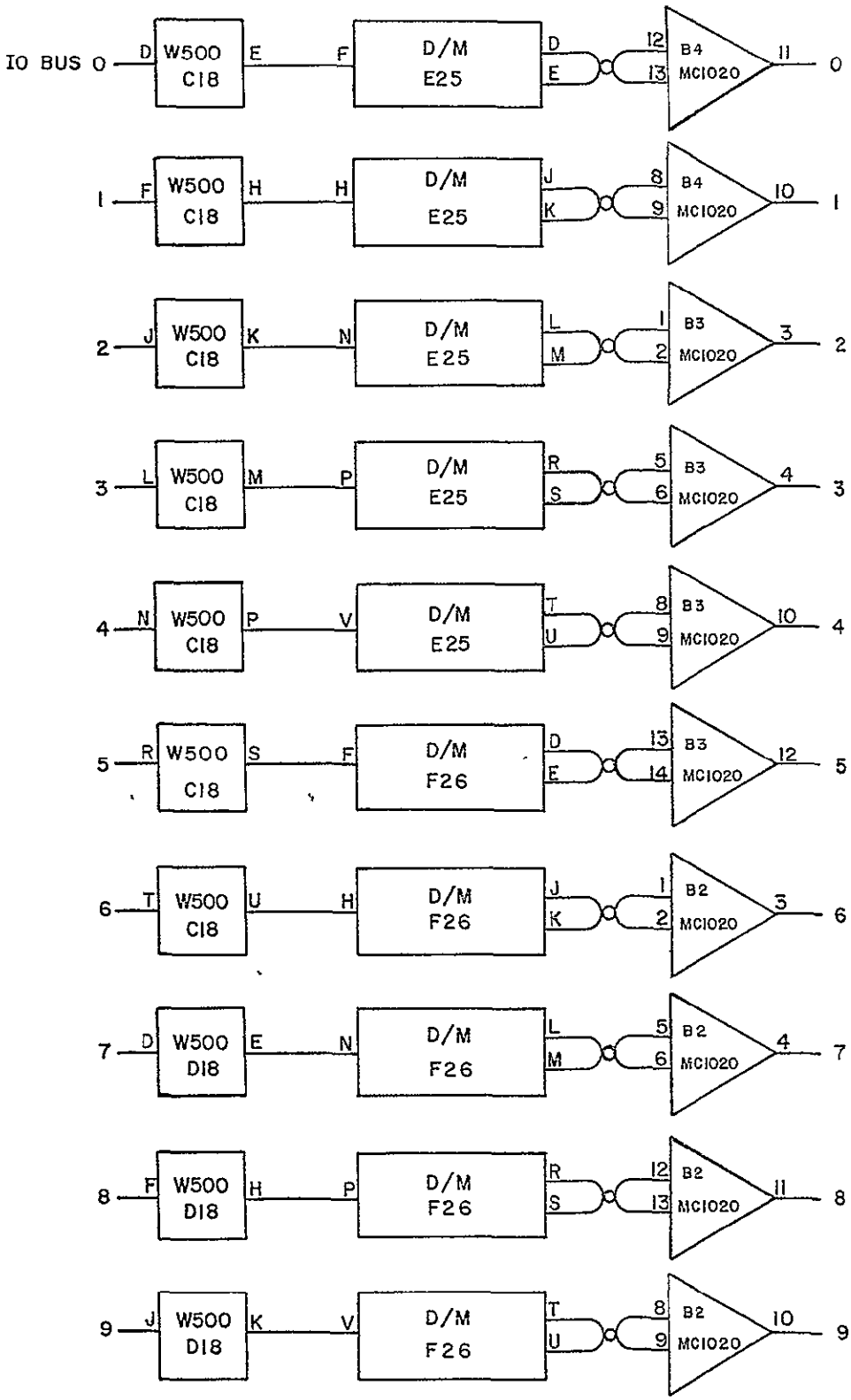


Fig. 14 AC Bit Trunks for Preset Counter

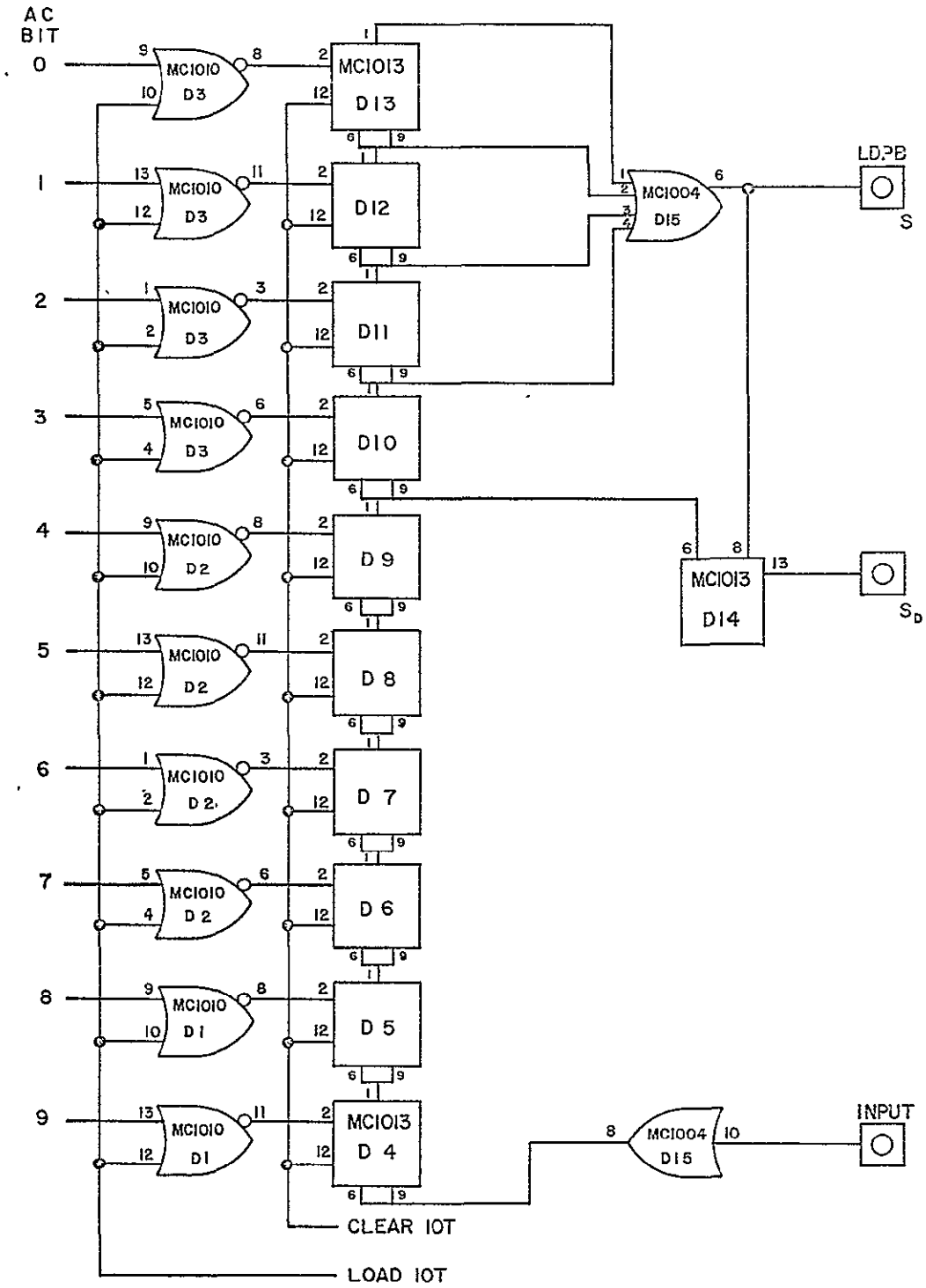


Fig. 15 Preset Counter Logic

Output of the data line emitter followers, AC 0 - 9, is converted to MECL levels and trunked to plug-in card B in the LOCUST digital patchbay. The data lines are brought to the counter card with ribbon cable. The clear IOT is obtained by gating IOT1 from a device selector with a subdevice bit. The load IOT is IOT2 gated with the same subdevice bit. Both counters use the same device selector. The different counters are selected with subdevice bits. IOT pulses are converted to MECL levels and brought to the counter card in the same manner as the data lines. The input, output, and delayed output lines are run from the counter card to card B with coaxial cable. Card B has direct connections to the digital patchbay.

The IOT1 pulse converted into a 100 nsec MECL "1" is used to reset (clear) the MC1013 J-K flip flops which make up the counter. A negative 100 nsec MECL "0" set pulse is gated with negative assertion data (a "1" in the AC is read out as a MECL "0" to the counter) to provide "1"s at the NOR output of the respective MC1010 set gates. The $\overline{Q}$ outputs of the counting flip flops are connected to the clock $\overline{C}_d$ input of the following flip flop. $\overline{C}_d$ is obtained by tying a $\overline{J}$ and $\overline{K}$ input together; MC1013 flip flops change state when a positive transition occurs at a $\overline{C}_d$ input. The input to the first counting flip flop is through a MC1004 OR gate to limit pickup which arises due to the short coaxial cable connection. The counter begins counting when input pulses appear. Patching must be done in the LDPB to prevent counting until desired.

The "S" pulse is obtained by gating the $\overline{Q}$ outputs of the four most significant bits of the counter with an MC1004 OR gate. These outputs all go to "0" 64 counts before all the $\overline{Q}$ outputs are "0"s. When the counter is full ($\overline{Q}$ outputs all "0") the next pulse causes all the outputs to go to "1"s. This causes a positive transition at a $\overline{J}$ and $\overline{K}$ input of the MC1013 flip flop used to generate "S_D". This flip flop was previously set to a "1" (Q output) when the counter was cleared. The positive transition at the $\overline{J}$-$\overline{K}$ input causes the output to go to a "0". The $\overline{K}$ input remains at a "1" while the $\overline{J}$ input goes to a "0" 32 input pulses later and back to a "1" 32 pulses after that. When the $\overline{K}$ input is a "1" and a positive transition occurs at the $\overline{J}$ input the flip flop output goes to a "1" until another positive transition occurs simultaneously at a $\overline{J}$-$\overline{K}$ input. Before that happens, the counter would usually be reloaded and another counting run begun.

Overload Light Reset Logic

A transistor switch was designed to provide power to the LOCUST overload lights. Since the lights latch on with SCRs when an overload occurs (Conant, 1968) it is only necessary to remove power from the latching circuit for 100 μsec to turn the SCRs off. The switching circuit is shown in Fig. 16. The control input (reset) to the switch is provided by either a patched negative transition in the LDPB or from the LOCUST mode-control switches.

A detector circuit is used to provide a MECL output whenever an overload occurs, i.e.,when an SCR anode voltage goes to 1 v. This

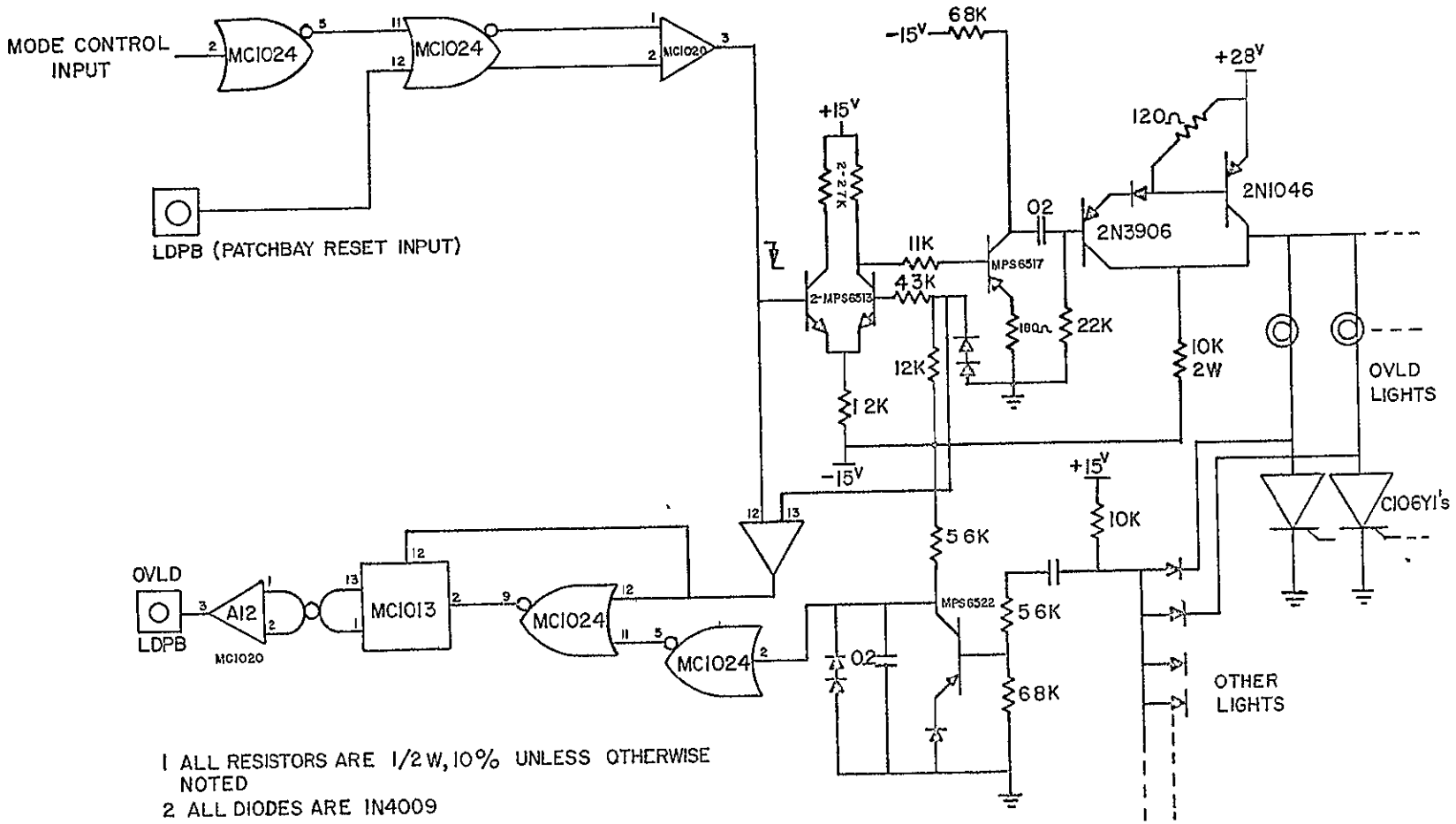


Fig. 16 Overload Light Logic

occurs during an overload or when the transistor switch is off. The detector circuit is also shown in Fig. 16.

An overload output in the LDPB indicates with a MECL "1" level whenever an overload occurs. The anode voltage detector output is gated with the reset input, and the result is used to set an MC1013 flip flop. The flip flop is reset with the overload reset input. The flip flop output in the LOCUST digital patchbay may be patched to one of the free flags to notify the PDP-9 of a LOCUST overload.

The MC1024 gates are in a single IC located on a card above the LDPB. All other logic is located on a card mounted behind the overload lights above the analog patchbay. There is only a single IC for each type of logic device used. The twisted pair connected to the MC1013 flip flop goes to the DEC logic where it connects with a twisted pair in the main trunk cable. This occurs on the output of D/M E26(S,R).

PDP-9 Internal Signals

The PDP-9 internal signals, IO RUN, ENABLE, IO SYNC, and IO POWER CLEAR, are converted to MECL levels and trunked to the LOCUST digital patchbay using the standard MECL trunking scheme.

Free IOT Pulses

The IOT pulses from a device selector are gated with subdevice bit 1 and converted to 1 μsec pulses using W640 pulse converters. They

are converted to MECL levels and trunked to the LOCUST digital patchbay. The wiring for this logic is not shown.

CHAPTER III

PATCHBAY AND IOT INSTRUCTIONS

This section describes the operation of the LOCUST/PDP-9 interface. The linkage terminations in the LOCUST digital patchbay and data-channel patchbay are discussed, and the associated PDP-9 input/output transfer instructions are given.

Patchbay points for the hybrid linkage are grouped in three columns in the LOCUST digital patchbay as follows:

1. ADC control inputs
2. DAC buffer-to-device transfer signals
3. Patchable flags
4. Data-bus read-in gates (used mainly to transmit status logic signal)
5. Six bit control register (receive digital control signals)
6. PDP-9 preset counters (used mainly as "alarm clocks")
7. Oscilloscope trunks for digital signals
8. Control signal trunks for data-channel interface
9. Overload signal
10. PDP-9 generated signals (clocks)
11. IOT timing and logic signals from the PDP-9

Interface terminations in the LOCUST digital patchbay are shown in Fig. 17. Interface terminations in the data-channel patchbay are shown in Fig. 18.

Linkage Patching

Patchable Flags

This group contains two flip flops connected to the I/O bus PI and Skip Request lines. A flag is UP when a MECL "1" is applied to its input in the LOCUST digital patchbay. Both flags may be tested with IOT instructions. They may be cleared by the CAF (clear all flags) command, the I/O POWER CLEAR signal, by the flag input going to a "0", or a programmable IOT pulse. The patchable flags can be used to interrupt the PDP-9 for conditions such as amplifier overload or a level change at a comparator output.

Analog-to-Digital Converters

The analog patchbay points for the converters are located to the left of the oscilloscope inputs. Proper patching is indicated in Fig. 19. Each ADC requires a LOCUST analog integrator/track-hold unit used for voltage-to-time conversion and two digital control signals from the digital patchbay, as shown. The analog input is patched to a TRACK input. Thus, the ADC performs its own sampling operation at the time the digital control signal goes to a "1".

Multiplying Digital-to-Analog Converters

Proper patching for a multiplying digital-to-analog converter is indicated in Fig. 20. Each MDAC requires an operational amplifier

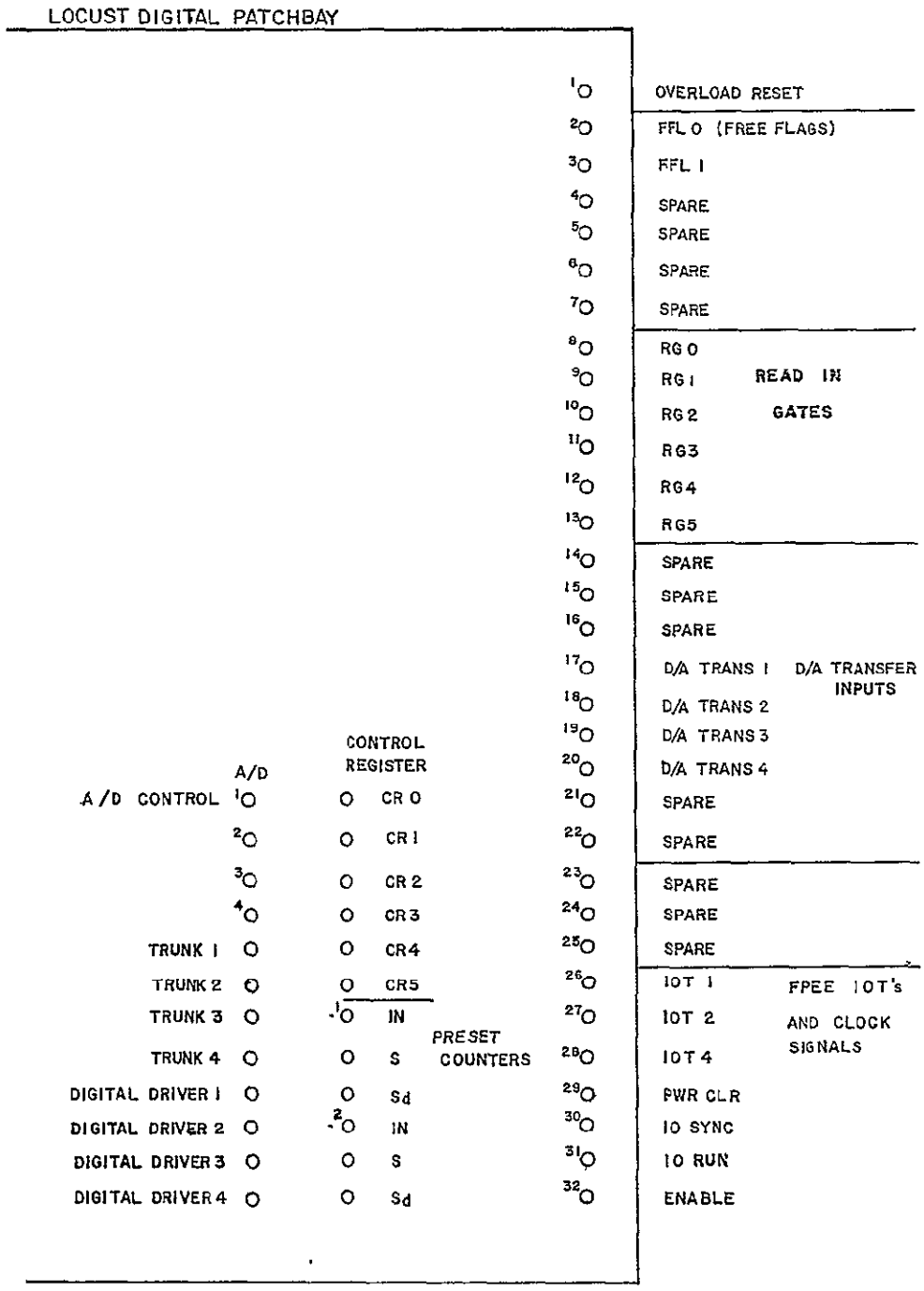


Fig. 17 Interface Patching in the LOCUST Digital Patchbay

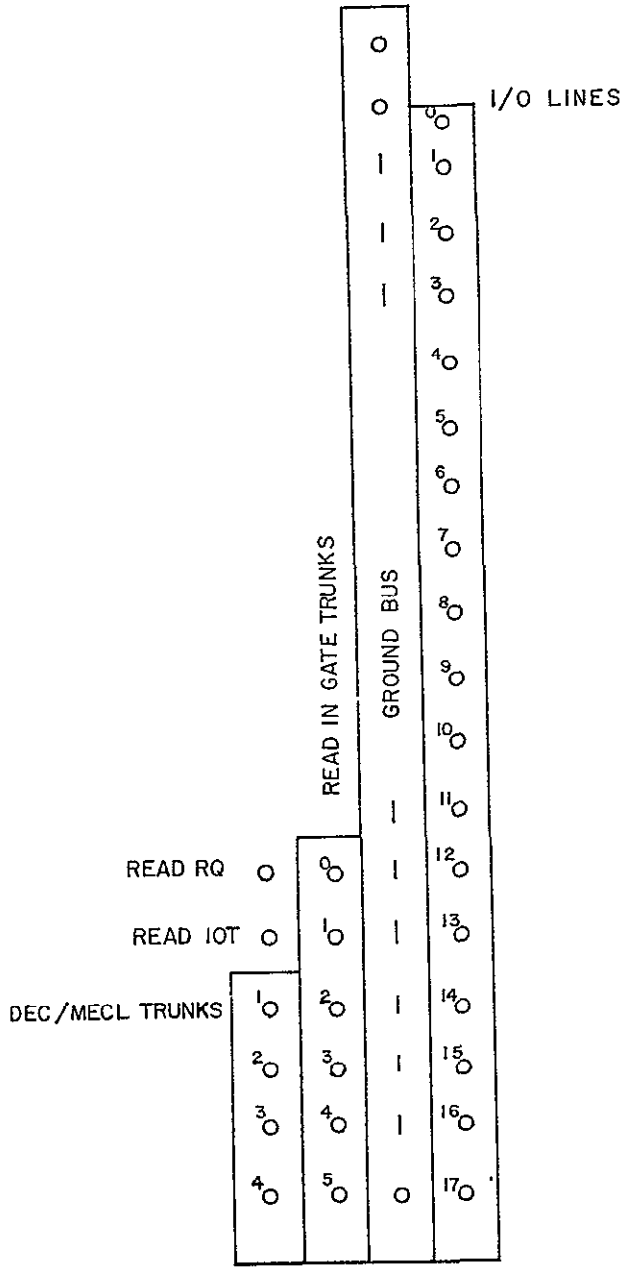


Fig. 18 Interface Patching in the Data-channel Patchbay

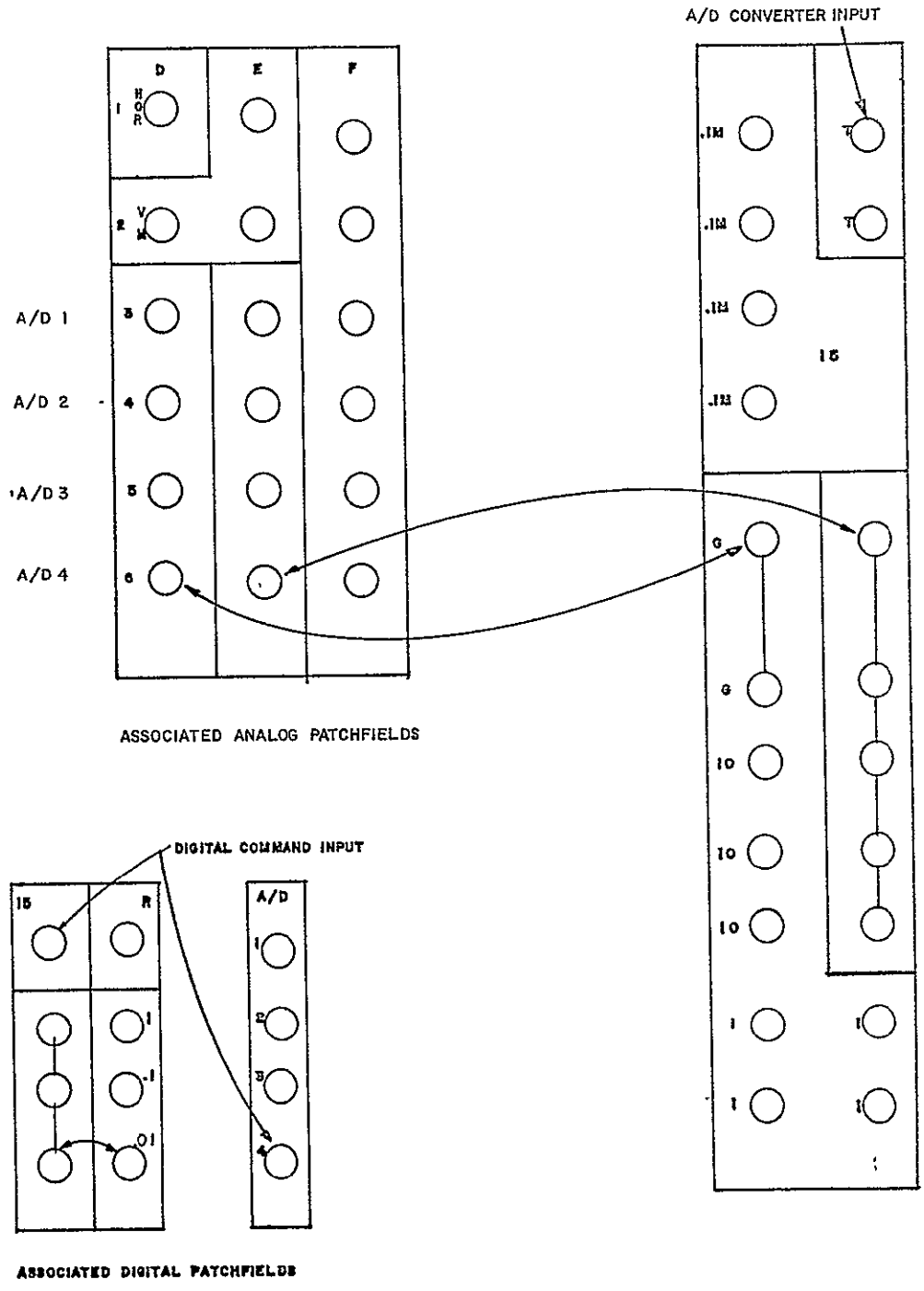


Fig. 19 A/D Converter Patching

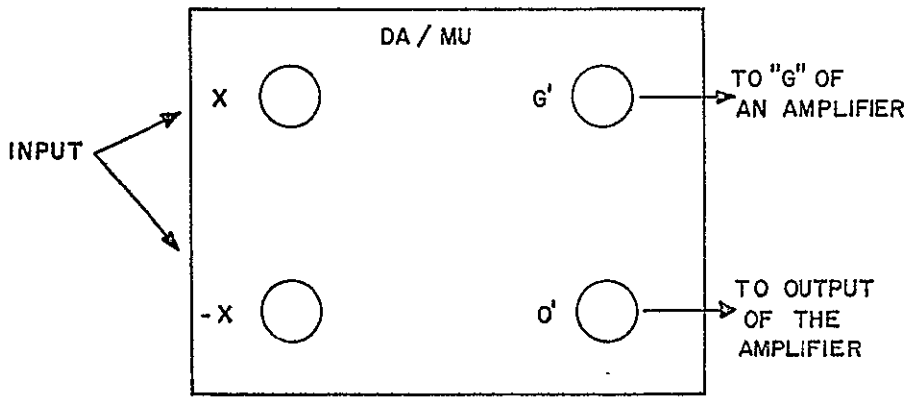


Fig. 20 MDAC Patching

without feedback. The MDAC buffer-to-device transfer inputs are located in the digital patchbay. A positive transition of at least 400 nsec applied to one of these inputs causes the transfer of the corresponding MDAC buffer register to its device register. These individual transfers can also be made under program control by the PDP-9.

Linkage Control Switches

The PI, SKIP, and ADC FLAGS toggle switches are located on the front panel containing the data-channel patchbay. The Program Interrupt switch connects all flags in LOCUST to the PDP-9 (PI) Program Interrupt line. The Skip switch connects LOCUST sense signals to the Skip Request line. The ADC FLAGS switch connects the ADC flags to the interface logic. For most interface operations all three switches would be ON. When operating LOCUST independently of the PDP-9, the PI and SKIP switches should be off to eliminate spurious signals on the interrupt and skip request lines.

Data-bus Read-in Gates

This group consists of inputs to 6 read-in gates which transfer data into the AC upon command. These inputs output as DEC levels in the data channel patchbay, where they must be patched to the desired accumulator lines. A MECL "1" in the LOCUST digital patchbay is read into the AC as a "1". To use the read-in gates patching

must be done in the LOCUST digital patchbay and in the data-channel patchbay, and the proper IOT signal must be given. The read-in gates are used for reading logic or "discrete" information such as analog computer states, and patchbay logic level into the PDP-9.

Six-bit Control Register

This double-buffered register is loaded with AC bits 0-5. A "1" in the AC is outputed as a MECL "1" in the LOCUST digital patchbay upon proper IOT command. The I/O POWER CLEAR signal clears the control register.

The control register allows the PDP-9, among other things, to control LOCUST'S mode. By patching between the control register output and the external mode control inputs in the LDPB, the INITIAL RESET, COMPUTE, or SINGLE RUN states of LOCUST may be selected. Mode control of individual integrators and control of patchbay flip flops may also be exercised.

Preset Counters

Two ten-bit counters located in LOCUST are loaded by the PDP-9. Each counter has an input, an output (S), and a delayed output (S_D) connection in the patchbay. AC bits 0-9 are loaded into the counters upon proper command. A timing diagram is shown in Fig. 12.

Oscilloscope Trunks

These trunks input in the LDPB and output with BNC connectors near the oscilloscope in LOCUST. The trunks are non-inverting.

Data-Channel-LOCUST Digital Patchbay Trunks

The inputs to these trunks are located in the data-channel patchbay. The ouputs, in the LOCUST digital patchbay, give a MECL "1" when the DEC input level is ground.

Overload Signal

The overload output remains at a "1" as long as any of the LOCUST amplifiers is overloaded. This output may be connected to a patchable flag to notify the PDP-9 of any overload condition.

PDP-9 Generated Signals

This group consists of four PDP-9 internal signals available on the I/O bus; I/O POWER CLEAR, I/O SYNC, I/O RUN, and ENABLE. The I/O RUN signal is present only if both I/O cables are plugged in.

Free IOT Signals

This group consists of the outputs of a special W103 device selector. The positive going IOT1, IOT2, and IOT4 signals are available in the LOCUST digital patchbay. These pulses may be used for many purposes, such as setting or resetting flip flops, initiating single runs, or clearing counters. Another use would be the resetting of LOCUST's overload lights.

Input/Output Transfer Instructions

This section defines the machine instructions and mnemonics which operate the ADCs, MDACs, and other devices which make up the LOCUST-PDP-9 interface. All linkage commands are defined here. A summary of linkage instructions is presented in Table I at the end of this section.

Patchable PI Flags

Two flag inputs are located in the linkage section of the LOCUST digital patchbay. A MECL "1" patched to either input causes a program interrupt. The PDP-9 uses a chain of skip instructions to determine the cause of the interrupt. When the interrupting device has been determined a service subroutine is executed. The patchable flags are tested by skip instructions.

MNEMONIC	OCTAL CODE	OPERATION EXECUTED
LSF1	701541	The next instruction is skipped if Free Flag #1 is set.
LSF2	701521	The next instruction is skipped if Free Flag #2 is set.
LCF1	703444	Clear Free Flag #1
LCF2	703544	Clear Free Flag #2

Analog-to-Digital Converters

The ADC flags are tested with PDP-9 skip instructions. The converter data is read into the AC and the device flag cleared with an IOT2 instruction.

MNEMONIC	OCTAL CODE	OPERATION EXECUTED
LAD1S	703441	The next PDP-9 instruction is skipped if ADC #1 flag is set.
LAD1R	703452	Clear the AC and load AC 0-10 with the contents of ADC #1 register. Clear ADC #1 flag.
LAD2S	703541	The next PDP-9 instruction is skipped if ADC #2 flag is set.
LAD2R	703552	Clear the AC and load AC 0-10 with the contents of ADC #2 register. Clear ADC #2 flag.
LAD3S	703641	The next PDP-9 instruction is skipped if ADC #3 flag is set.
LAD3R	703652	Clear the AC and load AC 0-10 with the contents of ADC #3 register. Clear ADC #3 flag.
LAD4S	703741	The next PDP-9 instruction is skipped if ADC #4 flag is set.
LAD4R	703752	Clear the AC and load AC 0-10 with the contents of ADC #4 register. Clear ADC #4 flag.

Multiplying Digital to Analog Converters

Data on the I/O bus data lines is strobed into MDAC buffer registers by the following instructions.

MNEMONIC	OCTAL CODE	OPERATION EXECUTED
LDA1C	703421	Clear MDAC #1 buffer register.
LDA1L	703422	Load MDAC #1 buffer register with AC 0-11.
LDA2C	703521	Clear MDAC #2 buffer register.
LDA2L	703522	Load MDAC #2 buffer register with AC 0-11.

MNEMONIC	OCTAL CODE	OPERATION EXECUTED
LDA3C	703621	Clear MDAC #3 buffer register.
LDA3L	703622	Load MDAC #3 buffer register with AC 0-11.
LDA4C	703721	Clear MDAC #4 buffer register.
LDA4L	703722	Load MDAC #4 buffer register with AC 0-11.

Data in a buffer register is jam-transferred into its device register by either an IOT instruction or by a MECL "1" patched into the proper D/A TRANS input in the LOCUST digital patchbay. The following instructions are used in buffer-to-device register transfers.

MNEMONIC	OCTAL CODE	OPERATION EXECUTED
LDA1X	703424	Transfer the contents of MDAC #1 buffer to device register.
LDA2X	703524	Transfer the contents of MDAC #2 buffer to device register.
LDA3X	703624	Transfer the contents of MDAC #3 buffer to device register.
LDA4X	703724	Transfer the contents of MDAC #4 buffer to device register.

Data-bus Read-in Gates

The six read-in gate inputs in the LOCUST digital patchbay have DEC outputs in the data channel patchbay. These outputs must be connected to DEC gate inputs corresponding to the desired accumulator bits. A read request must also be patched. The data

is read into the AC when the proper IOT instruction is given. A "1" patched in the LOCUST digital patchbay is transferred into the AC as a "1".

MNEMONIC	OCTAL CODE	OPERATION EXECUTED
LTR1	702212	Clear the AC and load AC bits selected in data channel patchbay with logic levels patched to read-in gates.

Six-bit Control Register

Data from AC 0-5 is transferred to the control register buffer and then jam-transferred to the output register. A "1" in the AC is a MECL "1" at the proper output in the LDPB. The output register may be cleared with I/O POWER CLEAR. The following IOT instructions are used for the control register.

MNEMONIC	OCTAL CODE	OPERATION EXECUTED
LCRC	701641	Clear buffer register.
LCRL	701642	Load buffer with AC 0-5.
LCRX	701644	Jam-transfer buffer contents into output register.

Preset Counters

The 10-bit preset binary counters are used to count LOCUST-generated pulses and issue two control pulses. The counter is loaded with the complement of one less than the number of pulses to be counted. The "S" output pulse is 64 input pulse widths wide and is a negative MECL pulse, whose positive transition occurs at the

end of a counting run (See Fig. 12). The "S_D" pulse is the same width as the "S" pulse but its positive transition occurs 64 input pulse widths after the end of a counting run. The counters are loaded from the PDP-9 and start counting as soon as input pulses occur. For "S_D" to be issued the input pulses must continue to occur for at least 64 pulses after the "S" pulse has been issued. There are two preset counters in LOCUST that are loaded from the PDP-9. The following instructions are used.

MNEMONIC	OCTAL CODE	OPERATION EXECUTED
LCN1C	701542	Clear counter #1
LCN1L	701544	Load AC 0-9 into counter #1
LCN2C	701522	Clear counter #2
LCN2L	701524	Load AC 0-9 into counter #2

Free IOT Signals

Three pulses are available from the PDP-9 which are outputed in the LDPB. The following instructions are used.

MNEMONIC	OCTAL CODE	OPERATION EXECUTED
LP1	701621	A 1 μsec pulse is generated at event time 1.
LP2	701622	A 1 μsec pulse is generated at event time 2.
LP4	701624	A 1 μsec pulse is generated at event time 3.

TABLE 1

IOT INSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION EXECUTED
LAD1S	703441	Skip if ADC #1 flag is set.
LAD1R	703452	Read ADC #1 and clear flag.
LAD2S	703541	Skip if ADC #2 flag is set.
LAD2R	703552	Read ADC #2 and clear flag.
LAD3S	703641	Skip if ADC #3 flag is set.
LAD3R	703652	Read ADC #3 and clear flag.
LAD4S	703741	Skip if ADC #4 flag is set.
LAD4R	703752	Read ADC #4 and clear flag.
LDA1C	703421	Clear MDAC #1 buffer register.
LDA1L	703422	Load MDAC #1 buffer register.
LDA1X	703424	Load MDAC #1 device register.
LDA2C	703521	Clear MDAC #2 buffer register.
LDA2L	703522	Load MDAC #2 buffer register.
LDA2X	703524	Load MDAC #2 device register.
LDA3C	703621	Clear MDAC #3 buffer register.
LDA3L	703622	Load MDAC #3 buffer register.
LDA3X	703624	Load MDAC #3 device register.
LDA4C	703721	Clear MDAC #4 buffer register.
LDA4L	703722	Load MDAC #4 buffer register.
LDA4X	703724	Load MDAC #4 device register.

TABLE 1 continued

MNEMONIC	OCTAL CODE	OPERATION EXECUTED
LSF1	701541	Skip if Free Flag #1 is set.
LCF1	703444	Clear Free Flag #1.
LSF2	701521	Skip if Free Flag #2 is set.
LCF2	703544	Clear Free Flag #2.
LCN1C	701542	Clear counter #1.
LCN1L	701544	Load counter #1.
LCN2C	701522	Clear counter #2.
LCN2L	701524	Load counter #2.
LCRC	701641	Clear control register buffer.
LCRL	701642	Load control register buffer.
LCRX	701644	Load control register output register.
LP1	701621	Issue IOT1.
LP2	701622	Issue IOT2.
LP4	701624	Issue IOT4.
LTR1	702212	Read LOCUST read-in gates.

CHAPTER IV

APPLICATION

The LOCUST / PDP-9 interface operation was demonstrated using a program written by Emmett Pearse O'Grady (O'Grady, 1969). This section is based on his dissertation and serves only to demonstrate hardware operations, not a novel program.

Amplitude Distribution Measurement Example

In many hybrid-computer applications we compute statistics of a random process (Korn, 1966). Averaging, correlation studies, and amplitude distribution analysis are typical examples. This section describes a program used to study the amplitude distribution of a voltage waveform available on the analog-computer patchbay. Our solution illustrates the use and programming of the program interrupt facility and demonstrates an interesting real-time display technique made possible by the program interrupt.

Statement of Problem

The problem can be stated as follows: given a voltage x(t) on the analog-computer patchbay with amplitude in the range $|x(t)| \leq 10$ volts, compute and display the amplitude distribution of x(t). The amplitude distribution curve is a histogram with equal-width class intervals which represent the voltage range $-10 \text{ volts} \leq x \leq 10 \text{ volts}$.

A suitably scaled amplitude distribution curve is an estimate of the probability density function of x(t).

Method of Solution

This problem involves both computing and displaying the amplitude distribution curve. The curve is computed in the form of a histogram with 400_8 equal-width class intervals; the column heights are stored in an array (400_8 memory locations) labeled HISTO. The histogram is computed as follows:

1. An analog-computer track/hold circuit samples x(t) and holds it for A/D conversion.
2. The sampled voltage is converted to digital form and read into AC 0-10, using the program interrupt facility. The eight most significant bits establish the class interval within which the sample falls and, when added to the address of the first memory location in the array HISTO, specify the address of the memory location holding the column height of that class interval.
3. The column height specified by the sample's class interval is incremented and step (1) is repeated.

The sampling process is repeated until the number of samples falling in any one interval equals 3777_8, the largest number that can be displayed by the MDACs. The curve is displayed with the aid of two MDACs as an X-Y oscilloscope plot. The X-MDAC output voltage sweeps through 400_8 states corresponding to the class intervals; the Y-MDAC

output voltage is proportional to the number of events falling within each interval. The X and Y MDACs are updated simultaneously.

A large percentage of the time required to compute the histogram is taken up by A/D conversions during which the digital computer is idle. By taking advantage of the PDP-9 program interrupt facility, our program uses this idle time to provide a dynamic display of the histogram as it builds up. The main program is a display routine which provides a complete display of the histogram approximately every 6.5 msec. This program is interrupted whenever the A/D converter completes a conversion, approximately every 100 μsec depending on ADC word length. Word length should be 8-bits or longer for best display. The total number of samples required depends on the amplitude distribution under study.

Figure 21 presents a flow chart of the solution procedure Table 2 lists the PDP-9 program, and Fig. 22 illustrates analog-computer patching.

Results

The method of solution described above was evaluated by obtaining amplitude-distribution curves for a square wave, a sine wave, a triangle wave, and for Gaussian noise. Figures 23 to 26 present typical curves obtained in each case; these curves agree in form with expected results.

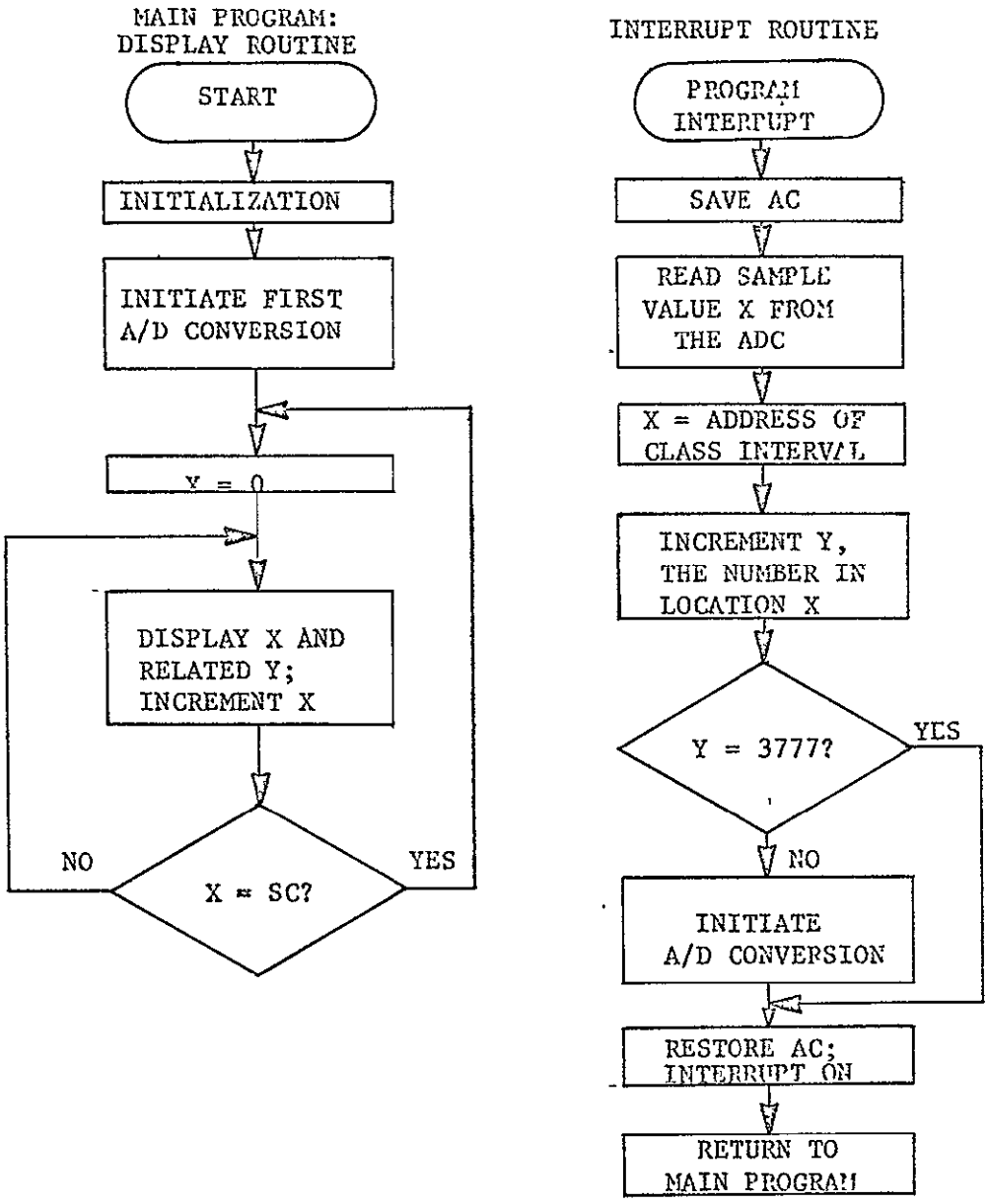


Fig. 21 Flow Chart for Amplitude-distribution Example

TABLE 2 HISTOGRAM

```
/THIS PROGRAM IS USED TO GENERATE A
/HISTOGRAM. DATA IS OBTAINED FROM THE
/ADC USING THE PROGRAM INTERRUPT FACI-
/LITY THE PROGRAM IS A MODIFICATION
/OF THE PROGRAM IN O'GRADY'S THESIS
/TO RUN ON LOCUST.
/
RESTR   NOP             /ALLOWS RESTART.
/
/INITIALIZATION ROUTINE
/
SETUP   CAL Ø           /SET UP HANDLER TO
        16              /SERVICE ADC#1 THRU
        7Ø3441          /PROGRAM INTERRUPT.
        A2DFLG
        DBK
        LAC (JMP TAG1) /ALLOWS RESTART TO
        DAC RESTR       /JMP AROUND SETUP.
/
TAG1    LAC (4ØØØØØ    /CLEAR, LOAD, AND
        7Ø1647          /TRANSFER CONTROL
                        /REGISTER BIT Ø
                        /TO PLACE A "1" IN
                        /EXT. CP TO START
                        /COMPUTE PERIOD.
/
        7Ø3452          /CLEAR ADC#1 FLAG.
/
        LAC (DZM HISTO) /CLEAR THE ARRAY
        DAC CLEAR       /LABELED "HISTO."
        LAW -4ØØ
        DAC COUNT#
CLEAR   XX
        ISZ CLEAR
        ISZ COUNT
        JMP CLEAR
/
        ION             /TURN PION.
/
/DISPLAY ROUTINE
/
BEGIN   DZM X#          /PREPARE FOR
        LAC (LAC HISTO)/DISPLAY OF BIRST
        DAC YLOC        /COLUMN OF HISTOG.
YLOC    XX              /GET VALUE OF Y.
        7Ø3623          /LOAD Y (MDAC#2)
                        /BUFFER REGISTER.
        ISZ YLOC        /COMPUTE NEXT YLOC.
```

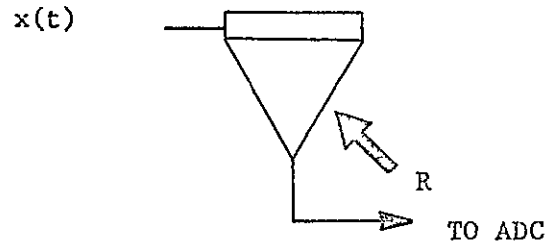
TABLE 2 continued

```
        LAC X           /GET VALUE OF X.
        703723          /LOAD X (MDAC#3)
                        /BUFFER REGISTER.
        703724          /TRANSFER X.
        703624          /TRANSFER Y.
        TAD INCRX       /COMPUTE NEXT X.
        SAD XMAX        /CHECK FOR X(MAX).
        JMP BEGIN       /REINITIALIZE
                        /DISPLAY
        DAC X           /STORE NEXT X.
        JMP YLOC        /START DISPLAY OF
                        /NEXT COLUMN OF
                        /HISTOGRAM.
/
/INTERRUPT ROUTINE
/
A2DFLG  DAC SAVEAC#     /SAVE AC.
        703452          /READ ADC#1.
        XOR SIGN        /ORDER THE COLUMNS
                        /(- TO +).
        CLL
        LRS 12          /DETERMINE WHICH
        TAD (HISTO)     /COLUMN F HISTOG.
        DAC TEMP        /TO INCREMENT.
        LAC* TEMP
        TAD INCRY       /INCREMENT IT.
        DAC* TEMP
        SAD YMAX        /CHECK FOR OVERFLOW
        JMP .+7
        LAC* (0)        /GET RETURN LOC.
        DAC RETURN#
        LAC SAVEAC      /RESTORE AC.
        ION             /TURN PI BACKON.
        DBR
        JMP* RETURN     /RETURN TO MAIN PGM

        LAC (0          /CLEAR,LOAD, AND
        701647          /TRANSFER "0" THRU
        JMP .-10        /CONT. REG. BIT 0
                        /TO BE COMPLEMENTED
                        /AND USED TO PUT
                        /LOCUST IN INITIAL
                        /RESET (EXT.IR).
/
/CONSTANTS
/
HISTO   .BLOCK 400      /RESERVE 400(OCTAL)
                        /LOCATIONS FOR
```

TABLE 2 continued

```
TEMP    Ø
INCRY   1ØØ
YMAX    377ØØ
INCRX   1ØØØ
XMAX    4ØØØØØ
SIGN    4ØØØØØ
        .END RESTR
```



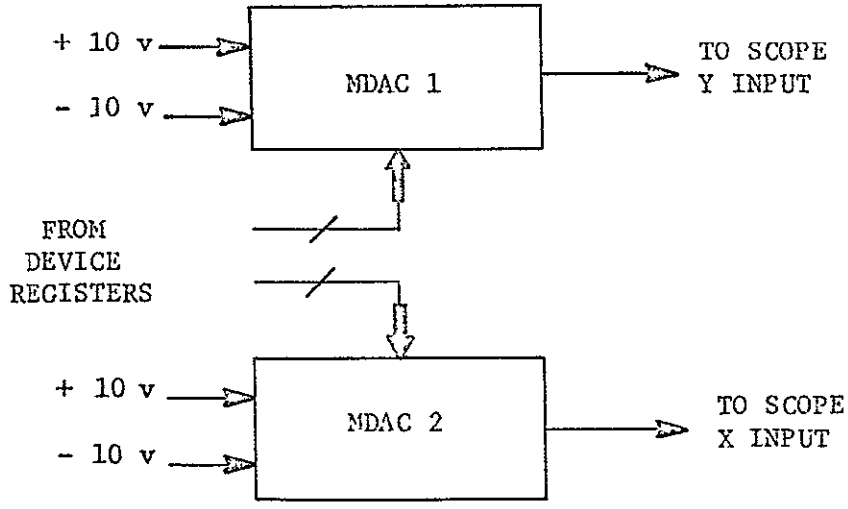
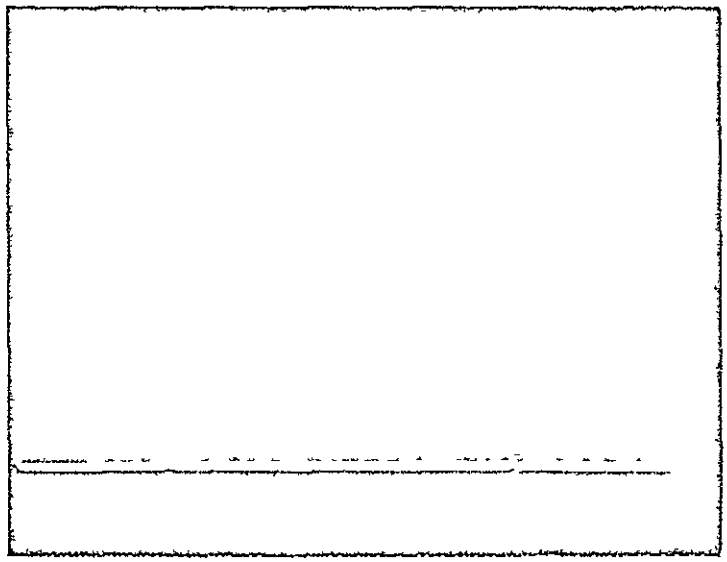
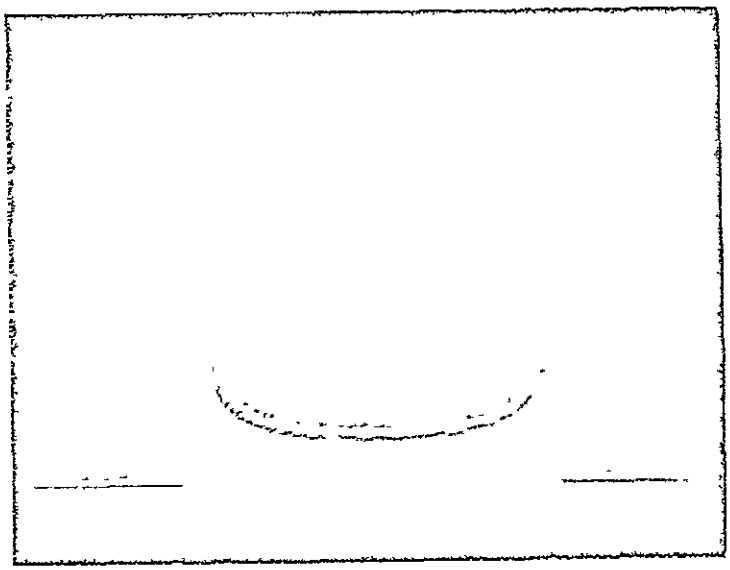


Fig. 22 Analog Patching for Amplitude Distribution Problem



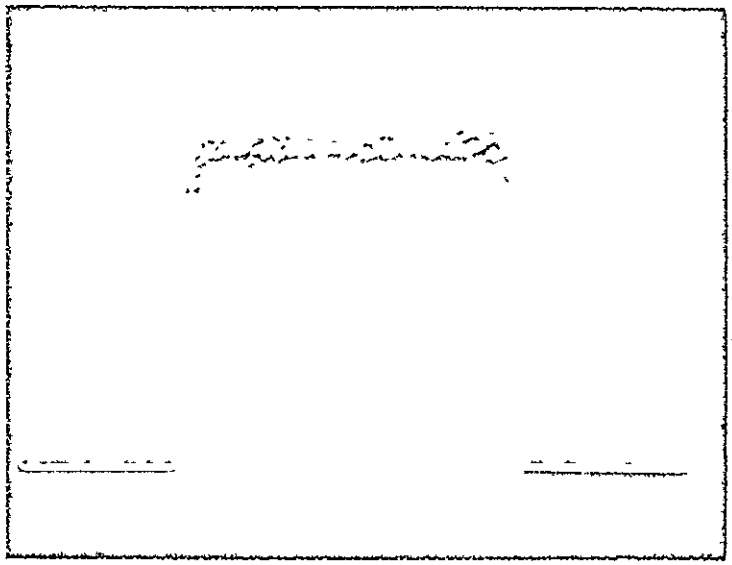
Vertical scale: 2 volts/cm
Horizontal scale: 1 volt/cm

Fig. 23 Amplitude Distribution of Square Wave



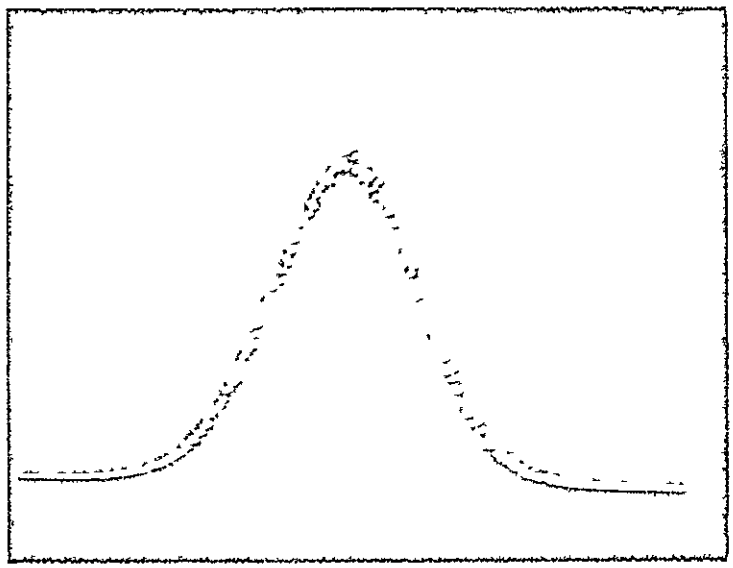
Vertical scale: 2 volts/cm
Horizontal scale: 1 volt/cm

Fig. 24 Amplitude Distribution of Sine Wave



Vertical scale: 2 volts/cm
Horizontal scale: 1 volt/cm

Fig. 25 Amplitude Distribution of Triangle Wave



Vertical scale: 2 volts/cm
Horizontal scale: 1 volt/cm

Fig. 26 Amplitude Distribution of Gaussian Noise

CHAPTER V

CONCLUSIONS

The design and test of the LOCUST/PDP-9 interface was completed with satisfying results. An application problem was run which demonstrated some of the data transfer and control capability of the interface. Noise measurements were made and it was found that the noise level in the analog patchbay, measured at the output of an unused amplifier, was not significantly increased by the addition of the interface. The peak noise level remains less than 5 mv.

It has thus been shown that it is possible to interconnect a digital computer with a high ambient noise level to a machine that uses fast integrated circuit logic operating with small logic level swing in a low noise environment. This is encouraging and suggests new opportunities of system additions to the PDP-9. Already a floating point arithmetic unit, built with MECL II, is being designed for the PDP-9.

In the process of designing and building an interface many desirable additional features become apparent. A faster analog-to-digital converter would be a welcome addition to the interface. Automatic Priority Interrupt (API) would also make the interface more powerful. A data channel interface, presently being built, will transfer data directly to and from the core memory of the PDP-9. This will greatly increase data transfer speed and save programming effort and storage. Future users will recognize needs and solutions to improve this hybrid combination.

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